INSTRUCTION MANUAL

DANBRIDGE
DENMARK

CDB 1

1MHz CAPACITANCE DEVIATION BRIDGE

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ADDENDUM TO INSTRUCTION MANUAL FOR CDB 1, CAPACITANCE DEVIATION BRIDGE

Change: PC Boards Nos. 18 and 16 - BGO-2 and GBT-2 changed to BGO-3 and BGT-3.

Correction to Detailed Circuit Description

Page 17 to 18. Par. 4.7.

Read: Diagram 12 - BGO-3, Board No. 18
Diagram 12A - BGT-3, Board No. 16.

Page 18, from second passage to end of paragraph 4.7.

Read: The preamplifier is an integrated amplifier (LM356) coupled in the inverting mode with high DC-gain. Its inverting input (a virtual earth point) functions as the summing point for the driving D-C current from the Main Detector and the feed-back current from the Balance Detector through the range switch.

An off-set control zeroes out voltage off-set at the input.

The amplifier output is coupled through a divider to the signal input of the MC1596.

The maximum output of the generator is limited to approximately 1.3 times the maximum required (more for the 90^{o} system)

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1. INTRODUCTION

The CDB 1 is a four-terminal capacitance deviation and loss-factor measuring system with a measuring frequency of 1MHz.

The four-terminal arrangement eliminates measuring errors due to lead impedance and contact resistance and makes it possible to measure capacitors in the range of .01pF to 11nF with an accuracy of 0.1% simultaneously with a loss factor down to 10^{-4}. The capacitance deviation may be measured in per cent or - for low value capacitors - in pF. The loss factor is measured directly (in %) or - again for low value capacitors - in equivalent parallel conductance.

The system consists of two modules: A 19" width module containing the electronics, the read-out meters and the range selectors and connected by coaxial cables to the smaller bridge module containing the bridge circuit, the standard capacitors and associated controls. This arrangement facilitates the use of the system in conjunction with automatic sorting equipment by making it possible to mount the bridge circuit close to the measuring point, thus reducing lead errors.

Analog outputs for both measured parameters are provided which can be used as input to a limit selection system - e.g. the Danbridge TLS System - controlling the sorting. The measuring system is auto-balancing, which means a constant measuring voltage across the unknown capacitor (within the selected range) and a very small measuring time.

SPECIFICATIONS

Measuring Frequency:	1MHz ±0.1%.
Capacitance Range:	Main range 0 to 1110pF, in %/tgδ mode 100 to 1110pF. Set on two decades with calibrated fine adjustment.
Range Multiplier:	x0.1, x1, x10.
Accuracy:	±0.1% of setting ±0.01% of range, on x10 range ±1% of setting.
Meter Display:	Choice of two modes. Mode 1: Capacitance deviation ΔC in %, range ±2, ±6, ±20, ±60 full scale. Loss displayed as tgδ, range 0.3, 1, 3, and 10% full scale.

Mode 2:
Capacitance deviation ΔC in pF, range ±2, ±6, ±20, and ±60pF full scale, scaled by range multiplier. Loss displayed as parallel conductance, range 2, 6, 20, and 60μS Gp, scaled by range multiplier.

Meter Display Accuracy:

Basic accuracy ±2% of reading ±1% of full scale. Additional inaccuracy for tgδ on x10 range up to ±1%.
Accuracy on 0.3% tgδ range ±0.01% tgδ ±3% of reading.
For Gp range additional errors proportional to setting of standard may appear, up to ±0.5μS at max. setting and scaled by range multiplier.

Measuring Voltage:

x0.1 range 3V, x1 range 300mV, x10 range 30mV.

Settling Time:

Max. 50 milliseconds.

Analog Outputs:

1V into min. 1kΩ external load for full scale meter deflection.

Terminals:

Four-terminal connection with separate earth terminals minimizes errors due to lead impedance and stray impedance to ground.
Detector and generator terminals are 4mm jacks with 19mm spacing to enable the use of standard component fixtures.
Test fixture residuals: Up to 5pF capacitance and 0.3μS conductance can be compensated by panel adjustments on the bridge unit.

Power:

100 to 130V and 200 to 260V, 50-60Hz, 30W.

Dimensions:

Main Frame:
19" rack, 260 (deep) x 133 (high) mm overall dimensions.

Bridge Unit:
235 x 140 x 120mm overall dimensions.

Total Net Weight:	10.5 kg
Accessories supplied:	One pair of fixture for axial-lead components. One fixture for radial-lead components. One power lead. One 7-pole connector for output cable.
Accessories available:	Test Limit Selector, Type TLS 1.

2. OPERATING INSTRUCTIONS

2.1. Setting Up

Check that the mains voltage selector is set to the actual supply voltage. The selector switch is located on the rear panel. To change the setting, pull the knob, turn to the correct position and push back.

Check that a 0.5A slow-blow fuse is fitted.

Connect the bridge module to the main frame with the five cables according to the number indications.

As a four-terminal bridge circuit is used, the two detector terminals and the two generator terminals respectively must be interconnected before any checks or measurements are possible. When using the test fixtures supplied by Danbridge the terminals are automatically interconnected. If other types of test fixtures are used the terminals must be shorted externally when checking.

Note that two sets of generator terminals are provided to enable measurements on capacitors of different lengths.

The upper terminals are the current terminals and for two-terminal measurements the unknown should be connected to these terminals with the shortest possible leads.

Two ground terminals are provided. These are placed between the detector and generator terminals so that a ground shield may be mounted if required. All terminals are jacks for 4mm banana plugs.

2.2. Initial Calibration

Set the Controls as follows:

On the Bridge Unit:

Multiplier	x1
Mode Switch	ΔC pF/Gp
Standard Capacitor Dials	Zero

On the Main Frame:

ΔC Range	2pF f.s.
Gp Range	2μS f.s.

Switch on the equipment and allow for at least 15 minutes stabilization before calibration.

Adjust the C_o knob on the bridge unit to zero reading on the ΔC meter.

Adjust the "Gp ZERO ADJ." potentiometer on the main frame to zero reading on tgδ/Gp meter.

Set multiplier to x0.1 range.

Adjust Gp_o on bridge module for zero on tgδ/Gp meter.

Switch to x1 range and readjust "Gp ZERO ADJ." on main frame.

If necessary, repeat above adjustments for correct zero reading on both ranges.

If, during measurement, another measuring fixture is used, check zero on x0.1 range and readjust C_o and Gp_o on bridge.

Change ΔC range to 20pF f.s.

Operate the switch "CHECK 20pF ΔC".

Adjust the "20pF ΔC ADJ." potentiometer to full scale reading on the ΔC meter, and

Adjust the "Gp/ΔC ADJ." for zero change of the Gp meter (other than transient).

If this calibration procedure is insufficient to obtain the stated meter readings, readjustment as described in the "Maintenance Instructions" of this manual may be necessary.

2.3. Measurement

2.3.1. Measurement by Balancing

Place the unknown in the measuring jig and set as follows:

On the Bridge Unit:

Multiplier switch so that reading will lie between 1 and 10 on the Standard x100pF decade

Mode Switch	ΔC%/tgδ
Standard Dials	Zero

On the Main Frame:

ΔC Range	60% f.s.
tgδ Range	10% f.s.

Rotate x100pF standard dial to obtain minimum reading on ΔC meter and set meter to zero by adjusting the x10pF and x1pF dials. Switch the ΔC range to 2% f.s. for accurate zeroing.

Switch tgδ range to maximum reading within scale.

Capacitance value is now read on the 3 standard dials multiplied by the Multiplier Setting.

Tgδ value is displayed on the tgδ meter with tgδ range switch indicating full scale value.

Note: For capacitance settings below 1 digit on the x100pF dial, the accuracy of the dial readings and the meter indications will decrease, and for very low settings the meter settling time will increase. Thus to obtain the highest accuracy do not use settings much below 1 on the x100pF dial (or 10 on the x10pF dial).

For lower settings it is preferable to use the pF/Gp mode. The capacitor loss will now be displayed as parallel conductance (μS) on the lower scales of the meter in conjunction with the range switch and multiplier settings.

2.3.2. Deviation Measurement

To measure an unknown capacitor's deviation from a nominal value set as follows:

Mode Switch	ΔC%/tgδ
Multiplier & Standard Dials	nominal value

ΔC and tgδ range switches to appropriate full scale values of expected maximum deviation and loss.

Connect the unknown and read ΔC% and tgδ% directly on the meters in conjunction with the meter range settings.

For low value capacitors, measurement of deviation in absolute values is preferable. In this case set the Mode Switch to ΔC pF/Gp. The meters now display capacitance deviation in pF and capacitance loss as parallel conductance in μS. Both readings must be multiplied by the Multiplier setting in addition to the scaling by the range switches.

Measurement Errors

Tgδ Error at high ΔC Deviation

At ΔC deviation above 20%, errors in tgδ display up to ±0.05% absolute may appear so that, for accurate measurements of small tgδ values, ΔC must be less than 20%.

Errors due to external Ground Capacitance

When external measuring jigs are connected to the measuring terminals, additional ground capacitances are introduced, especially if long shielded cables are used. These capacitances give an error, especially any capacitance to the generator terminals.

The error is largest on the x0.1 range, where a 20pF capacitance gives a 0.1% high capacitance reading and about 0.01% high tgδ reading. On the x1 range 100pF ground capacitance gives the same errors.

To minimize this error and also errors due to small imperfections in the compensating circuit the shortest possible external leads should be used and, especially on the x0.1 range where series impedance is unimportant, low capacitance cable may be used.

For measurements on the higher capacitance values and cable lengths above 20cm please consult Danbridge.

Note on Gp Reading

In the ΔC pF/Gp mode the loss in the measured capacitor is expressed as an effective parallel conductance Gp. This is the reciprocal value of the effective parallel resistance Rp ($Gp = \frac{1}{Rp}$). The unit of conductance is termed Siemens (S) ℧, or mho.

The expression of loss as a conductance is in many cases convenient e.g. when calculating the loss in a tuned circuit comprising several components, as the total conductance is obtained by simply adding up the various conductances.

At low Gp values the stated tgδ accuracy of ±0.01% corresponds to an inaccuracy in Gp reading proportional to the setting of the standard and increasing to about ±0.6μS at maximum setting and scaled by the range multiplier setting.

3. PRINCIPLE OF OPERATION

3.1. The Bridge System

Diagrams 1 & 4

The bridge ciruit is a ratio-transformer design with a calibrated variable capacitor serving as the standard.

The bridge supply is obtained from the main circuit via a coupling transformer.

The three capacitance ranges are obtained by changing the transformer ratios.

The detector output from the junction between the standard and the unknown is fed to a low-impedance input on the main circuit.

When measuring within the meter ranges the bridge is automatically balanced, and the detector output is practically zero. The automatic balance is obtained by feeding a balancing voltage back from the main circuit into the bridge circuit.

A two-position switch ($\Delta C\%/tg\delta$ - ΔC pf/Gp) provides two modes of operation. In one position the balancing voltage is applied in series with the ratiotransformer voltage to the standard.

In the second position the balancing voltage is switched through a fixed capacitor to the detector junction.

A compensating circuit in the bridge compensates errors due to lead impedance at the unknown, thus providing true 4-terminal measurement.

3.2. The Measuring System

Diagrams 1 & 4

The Oscillator supplies the measuring voltage to the bridge circuit via the GEN. coax. Socket. The Oscillator is amplitude controlled by feed-back from the bridge via the REF. Socket, the Refence Input Amplifier and the Amplitude Detector. The action of this loop will keep the voltage across the unknown capacitor constant. The output from the Reference Input Amplifier - also constant - produces the Basic Reference Signal for the measuring system.

The difference in capacitance (ΔC) and loss factor ($tg\delta$) between the unknown capacitor and the standard, which is to be measured, is equivalent to the amplitude and phase angle (with respect to the measuring voltage i.e. the Basic Reference) of the difference or error voltage at the junction point between the two capacitors. Actually the error-current from this point into the low impedance Detector Input Amplifier is measured.

This amplifier's output is a voltage proportional in amplitude to - and in phase with - the error current into the DET. terminal. The output voltage is fed to the Main Detectors. These are amplitude detectors supplied with two reference signals from the reference system.

The reference signals are squarewave signals exactly in phase with - and 90^{o} out of phase with - the Basic Reference Signal and hence the measuring voltage in the bridge circuit. They are generated in two phase-locked loops described later (3.3.).

The Main Detectors will thus measure the amplitude of the 0^{o} and 90^{o} phase components of the error current, corresponding to the deviation in respectively loss factor and capacitance value of the unknown capacitor from the standard.

The output DC signals of the Main Detectors drive a balancing system (described later (3.4.)). This generates at the BAL. output terminal a voltage which is the vector sum of 0^{o} and 90^{o} phase signals precisely proportional in amplitudes to the respective Main Detector outputs.

This balance signal is applied to the balancing transformer in the bridge circuit (or through a fixed capacitor to the detection point) compensating any unbalance created by the difference between the unknown and standard capacitors. The whole system thus constitutes an auto-balancing bridge by virtue of the negative feed-back action from the detection point through the Main Detectors and the balance signal generating system to the balance transformer. Owing to the strict proportionality between the balance signals' phase components and the output DC voltages of the Main Detectors, these DC voltages are a measure of the balance signal necessary to keep the bridge in balance and hence of the difference between the unknown and the standard capacitors.

In the $\Delta C\%/tg\delta$ mode the balance signal is applied through the ratio transformer to the standard capacitor, and in this case the ΔC main detector output is displayed on the ΔC meter as the capacitance deviation in %. The $tg\delta$ Main Detector output is simultaneously displayed indirectly on the $tg\delta$ meter as the loss factor $tg\delta$. However, as the required balancing voltage for a given $tg\delta$ is proportional to the measured capacitance value, the $tg\delta$ detector output will depend on the ΔC value. To correct this error the detector output is put through an analog multiplier connected as a divider. This divides the $tg\delta$ detector output by the quantity $1 + \Delta C$ (%), thus giving an output voltage proportional to the loss factor $tg\delta$, which is then displayed on the $tg\delta$ meter.

In the pF/Gp mode the balance signals are applied to the detection point through a fixed capacitor, and the ΔC meter will display the capacitance deviation in pF, while the $tg\delta$ meter will display the effective parallel conductance Gp.

In this mode the divider correction is not required and is switched off so that the multiplier functions simply as a DC amplifier.

In order to check the calibration of the system a calibrating circuit is provided

This injects a current into the detector input corresponding to a 20pF ΔC deviation with zero $tg\delta$. This permits full scale ΔC meter calibration and zero phase angle calibration.

3.3. The Reference System

Diagram 2

The 0° and 90° reference squarewave signals for the main- and balance detectors are generated in two phase-locked loops (PLL).

The reference signals must have precise phase relations to the Basic Reference and must also fulfil the requirements of the detectors for which they serve as reference signals.

The detectors are designed around the monolithic MC 1596, a double balanced modulator/demodulator device (see f.ex. diagram No. 11) which gives an output as a product of an input signal voltage and a switching function. To minimize output errors in the detector, resulting from DC unbalance currents in its two branches, the duty cycle of the switching reference must be kept as close to 50% as possible.

Further, to avoid errors resulting from off-set voltages at the switching input terminals, the rise and fall times must be kept as small as possible. The squaring amplifiers (see description 4.6.) deliver the required precise squarewaves and the phase-locked loops, of which they are parts, secure the correct phases.

The 90° loop consists of an amplifier with the gain x2 $<-45^{\circ}$ which feeds one of the inputs of the squaring amplifier where a filter gives a further phase lag of 45°. The squarewave reference output is compared in phase to the Basic Reference Signal in the Phase Control Detector which in turn controls a voltage-controlled gain (VCG) amplifier. The loop is closed by the output of this amplifier being fed into the other input of the squaring amplifier supplying it with a 0° phase-correcting signal.

The 0^{0} phase-locked loop is rather similar though the Basic Reference Signal is used directly as input to the squaring amplifier. The phase-correcting signal must then be approx. 90° out of phase with the first input and the VCG amplifier has therefore an integrating filter in its input. The Phase Control Detector compares the phase of the 0° reference signal to the 90^{0} reference signal and thus locks the two reference signalphases to each other.

Both reference phases are therefore adjusted together, with respect to the Basic Reference Signal, by the front panel potentiometer "Gp/ΔC ADJ." which controls a small off-set current to the phase control detector in the 90^{o} PLL.

The denomination of this control reflects the fact that the Gp reading will vary with the capacitive deviation if the reference phases are misadjusted to the bridge voltage phase.

3.4. The Balancing System

Diagram 3

This system consists of two loops generating the 0^{o} and 90^{o} components of the balancing signal. The 0^{o} loop consists of a DC amplifier controlling an amplifier with voltage controlled gain. This amplifier is fed by the Basic Reference Signal and its output-current is fed to the Output Amplifier. The balancing signal is monitored by the Balance Detector which uses the 0^{o} reference squarewave signal as its reference, thus measuring the amplitude of the 0^{o} component of the balance signal. The detector's DC output is fed back through the range switch to the DC-amplifier input which thus becomes the summing point of the loop, because the loop is driven by a current from the Main Detector to this point.

Owing to a large forward gain the loop gain will be determined solely by the fixed and stable gain of the balance detector and the range switch thus maintaining a good proportionality between the Main Detector output voltage and the balance signal amplitude.

The 90^{o} balance loop is similar to the 0^{o} loop and shares the output amplifier with it. It has a zero controlling input to the balance detector set by a front panel mounted potentiometer "Gp ZERO ADJ.".

4. DETAILED CIRCUIT DESCRIPTION

4.1. The Oscillator

Diagram 5 - OSC-2 (PC Board No. 1)

The Oscillator is designed around the LM 271 (a monolithic single-stage differential RF amplifier) and a tuned circuit.

One of the output collectors feeds the tuned circuit and a separate winding on the same core delivers the positive feed-back signal to the base of the current-supplying transistor in the amplifier. The current through the differential pair is thus modulated and fed through the common base stage to the output.

The two transistors of the differential pair divide the signal current between them and thereby provide a means of gain control.

One of the inputs to the differential stage is biased by a zener reference and the other is reffered to two external controlling voltages, one from the Amplitude Detector (ODA-2 PC Board No. 3) and the other from the amplitude control potentiometer on the front panel ("20pF ΔC ADJ.").

The oscillator output must be a very pure sine-wave to avoid measuring errors due to odd harmonics. To achieve this a high-Q tuned circuit (Q about 200) is employed. This also ensures a good frequency stability, this being determined mainly by the components of the tuned circuit. A Darlington-coupled output amplifier minimizes loading of the oscillator.

4.2. The Amplitude Detector

Diagram 6 - ODA-2 (PC Board No. 3)

In order to keep a constant voltage across the unknown capacitor when the bridge balance varies the Oscillator's output amplitude must be controlled.

The reference point in the bridge, i.e. the generator terminal of the unknown capacitor, is monitored by the Reference Input Amplifier. The amplifier output - the Basic Reference Signal is fed to the Amplitude Detector which in turn controls the Oscillator's output amplitude. The detector is designed with a monolithic differential detector (MC 1596) and an operational amplifier (LM 301A).

The MC 1596 performs the amplitude detection by being supplied with the input signal to both the switching input (upper ip) and the signal input (lower ip).

The output, smoothed by the 1nF capacitors, delivers a current (differentially), proportional to the signal amplitude, to the inputs of the operational amplifier for voltage level-shifting and amplification.

The resistance network (the MC 1596 output collectorloads and the LM 301A gain setting resistors) consists of selected resistors, matched in value to less than 0.1% and in temperature coefficient to less than 5ppM/C^{o} in order to reduce common mode and temperature errors in the output voltage.

A multiturn cermet potentiometer with associated network provides nulling and off-set control.

The inputs are RF decoupled by series resistors (100Ω) and parallel capacitors (150pF).

4.3. The Reference Input Amplifier

Diagram 7 - AAC-2 (PC Board No. 5)

This amplifier's input is connected through the input BNC socket "REF" to the reference point in the bridge. Its output is the Basic Reference Signal for the measuring system with a constant 0.3V RMS amplitude. The amplifier is essentially an emitter follower with current feed-back for very low output impedance and bootstrapping to the input for high-input impedance. The transistors T1 & T2 are connected in a Darlington configuration for high current gain and T3 reduces the current swing in T2 thus reducing the output resistance to below 1Ω. Both input and output have an RC network in parallel to dampen out HF oscillation stemming from the long-lead reactances.

4.4. The Phase Correction Generators

Diagrams 8 & 9 - GEA-2 & AGE-2 (PC Boards Nos. 6 & 7)

These generators are part of the phase control loops which keep the two reference squarewaves in the correct phase relationships to the Basic Reference. They are driven by the phase detectors (PDO-2 & PDT-2) and deliver the error signals to the summing points (i.e. inputs of the squaring amplifiers (SQO-2 & SQT-2)) of the loops.

The generator boards are similar but board 7 (AGE-2) also contains a 45^{o} phase shifting amplifier for the input signal to SQT-2.

The generators are built around the MC 1596 integrated modulator/detector circuit. A small signal (20mV pp) derived from the Basic Reference by attenuation (and integration in the GEA-2) is supplied to the modulation (switching-) port (pin 8 diagram 8).

If the DC currents which supply the emitters of the balanced modulation transistors are equal no signal appears at the outputs but if the currents are different, signals opposite in phase and proportional in amplitude to the current difference appear. The current difference is controlled by a DC voltage at the input pin 1. (This DC voltage is the error voltage output from the Phase Control Detector).

One of the output collectors of the circuit drives an output emitter follower.

An offset control network with a cermet multiturn potentiometer is connected to the DC input terminal. The potentiometer is set when the loop is established, so that the Phase Detector output is zero and hence the correct phase between the reference squarewave and the Basic Reference is obtained.

The 45^{o} phaseshift amplifier on AGE-2 has a gain of approx. 2 and a phaseshift of approx. 45^{o}. Its input signal is the Basic Reference Signal and its output supplies the main input of the squaring amplifier SQT-2 (90^{o}) in which an RC network gives a further 45^{o} phaseshift to the signal, giving an overall phaselag of approx. 90^{o}. The fine phase tuning is obtained as in GEA-2 with the DC control potentiometer connected to the DC input of the AGE-2.

4.5. The Squaring Amplifiers

Diagram 10 - SQO-2 & SQT-2 (PC Boards Nos. 8 & 9)

The circuits are similar and supply the reference squarewaves to the main- and balancing detectors.

In order to minimize the effects of off-set voltages in the switching inputs of - and current unbalances in - the detectors, these squarewaves must have rise- and falltimes as small as possible and duty cycles as close to 50% as possible.

The amplifier is designed as a three-stage, non-saturating, switching amplifier. The first and second stages are designed with the LM 271 monolithic differential amplifier. The third stage is an emitter follower output stage with local current feed-back. This secures a very low output impedance in order to avoid any degrading of the rise- and falltimes by capacitive loading.

One of the first stage inputs is fed by the Basic Reference Signal (or, for the SQT-2, a signal derived from this by phase shifting it 45^{o} in the phase shift amp. on AGE-2 and further phase shifting it 45^{o} in the SQT-2 input).

The other input is fed by the phase error signal from the Phase Correcting Generator. Collector loads of 1kΩ are used in the first stage for high gain, and the output is clipped with diodes to avoid saturation.

The output signal is coupled capacitively to the second stage. The collector loads of this are split in two resistors each with a signal decoupling between. The signal load is low (50Ω) preserving the low rise- and falltimes. The signal amplitude is controlled at the second stage by a potentiometer which can vary the current through the bias chain to the current-setting transistor. The signal is capacitively coupled to the output stages to avoid influence on the collector DC voltages by the bias currents to the output emitter followers.

These DC voltages are important because the DC voltage differential between the decoupling points is proportional to the duty cycle. This difference voltage is fed to an integrated amplifier (LM 301A) for amplification and level shifting to ground potential.

One of the input bias networks of the input stage is returned to the DC amplifier output instead of ground, so that the DC amplifier controls the input bias point and effectively counteracts any deviation in the duty cycle (50%).

The duty cycle is set by a potentiometer controlling the off-set in the DC amplifier.

4.6. The Detectors

Diagram 11

The six detectors, i.e. the two Phase Detectors PDO-2 & PDT-2 (PC Boards Nos. 10 & 11)

the two Main Detectors MDC-2 & MDT-2 (PC Boards Nos. 13 & 12)

and the two Balance Detectors DBO-2 & DBT-2 (PC Boards Nos. 14 & 15)

are rather similar and only one, the MDC-2 will be described here in detail.

The Main Detector MDC-2 (for capacitance deviation)

The Detector is designed with the monolithic balanced modulator/ detector MC 1596.

The inherent stability of an IC makes it well-suited for the job.

To bias it and enhance its performance the following circuits are added. A 5.62kΩ resistor to pin 5 sets the DC currents in the two branches to approx. 1.2mA. The lower differential inputs - the signal port - are biased with two resistor networks, one of them variable to balance the DC currents through the transistors. This balancing is done (at the factory) by off-setting the duty cycle of the switching

signal applied to the upper (-switching) input, and observing the differential current output. If this stays unchanged the DC currents are balanced.

The 562Ω resistor between pin 2 and 3 (i.e. the emitters of the input transistors) sets the transadmittance of the signal stage.

The switching inputs are supplied with the squarewave reference (in this case the 90^{o} reference as the ΔC main detector is to detect a voltage derived from the unbalance current between the unknown and the standard capacitor in the bridge).

The outputs (the cross-coupled collectors of the switching transistors) are current-feeding an integrated amplifier (LM 301A) which adds gain and shifts the voltage level to ground potential.

The collector resistors (10kΩ) are matched to within 0.1% and to within 5ppM in temperature coefficient as are the feed-back and non-inverting input bias resistors of the amplifier, in order to reduce offset and temperature drift at the inputs of the amplifier.

A balancing network is further applied to the collectors (2x147kΩ & 10kΩ potentiometer) to increase common mode rejection. The potentiometer is (factory-) set to keep the output constant when varying the current into pin 5 of the MC 1596 and thereby the DC currents through the device.

The 0.1μF capacitors decouple the AC components of the collector currents and the 1μF feed-back capacitor (and the 1μF decoupling of the non-inverting input) sets the first pole for the detector and thereby for the whole auto-balancing loop of the bridge.

The collector differential voltage is diode-limited to reduce recovery-time after overdrive.

The output is likewise limited with diodes.

A potentiometer with associated resistors provides offset nulling.

The other detectors differ only in details like time constants and gain. The PDO-2 Phase Control Detector which compares the phases of the two reference squarewaves, uses differential signal input and DBO-2 and DBT-2 have a potentiometer in series with a resistor between pin 2 and 3 for precise gain setting.

The PDT-2 has an additional offset control from a frontpanel potentiometer "Gp/ΔC ADJ." so that adjustment of the squarewave reference system's phase with respect to the Basic Reference can be made easily.

Likewise the DBT-2 Balance Detector has a frontpanel offset adjustment "Gp ZERO ADJ." to zero out offsets created by residual temperature drift in the detector and in the 90° balancing generator BGT-2.

4.7. The Balance Generators

Diagram 12 - BGO-2 & BGT-2 (PC Boards Nos. 18 & 16)

These circuits, driven by the main detectors, generate the 0° and 90° components of the current which in the Output Balance Amplifier BOA-2 is converted to the balancing voltage delivered to the bridge circuit. This output voltage is detected by the Balancing Detectors DBO-2 and DBT-2 whose DC outputs in turn are fed back through the range selectors to the inputs of the generators. The gain and stability (i.e. of the ratio of the balancing voltage to the main detector voltages) is thus dependant only on the Balance Detectors (and the range selectors) and not the generators and the output amplifier which would not be stable enough.

The generators employ the MC 1596 modulator/detector as the VCG element in the same fashion as the Phase Correction Generators AGE-2 and GEA-2.

They are rather similar and only the BGO-2 (0°) will be described here.

The MC 1596 has as signal input the Basic Reference which is attenuated by a Wien bridge circuit to a 10mV peak signal compatible with the small linear range of the Switching input (pin 8). The Wien bridge circuit (low Q) allows an easy compensation by the 1kΩ potentiometer of the phase delay through the device.

The BGT-2 has a passive integrating divider (R-C) to attenuate and phase shift the Reference Signal approx. 90° and no provision for phase control. Its phase error is compensated in the output amplifier BOA-2 which it shares with the BGO-2 and the resultant phase error for the 0° balancing system must then be compensated at the signal input of the BGO-2.

The MC 1596 in fact functions as an AM modulator with a 1MHz carrier (the Basic Reference) and the DC signal from the preamplifier as modulating signal to the signal input (pin 4).

The preamplifier is an integrated amplifier (LM 301A) coupled in the inverting mode with high DC-gain. Its inverting input (a virtual earth point) functions as the summing point for the driving DC current from the Main Detector and the feed-back current from the Balance Detector through the range switch.

Both inputs to the amplifier have offset control. The one to the inverting input provides the bias current to avoid current offset errors with the different resistors in the range switch, and the other zeroes out voltage offset at the input.

The output of the amplifier is limited by diodes and coupled through a divider to the signal input of the MC 1596. This coupling network limits the maximum signal output from the generator to approx. 1.3 times the maximum needed (more for the 90^{o} system).

4.8. The Balance Output Amplifier & The Detector Input Amplifier

Diagram 13 - BOA-2 & DAA-2 (PC Boards Nos. 17 & 19)

The two amplifiers are similar in design and only the DAA-2 will be described here.

The amplifier employs the monolithic video amplifier MC 1552 as a preamplifier using its low impedance first-stage emitter as input terminal (pin 3).

The preamplifier's output is coupled to an L-C filter tuneable with a small trimmer for correct phase-setting. The filter has a Q of about 20 and its main purpose is to stop third harmonics generated in the Oscillator from reaching the Main Detectors.

The filter is connected to the two-stage output amplifier having a Darlington common emitter gain-stage and a totem pole output stage with local current feed-back.

This feed-back functions by sensing the current-swing in the emitter follower (at its collector load) and feeding this signal to the base of the lower transistor of the output complex. This transistor will then supply most of the output current thereby reducing the current-swing in the emitter follower and hence the output resistance to well below 1 Ohm.

A voltage feed-back for the output amplifier is provided for good phase stability and low input impedance. There is a limiting feed-back around the whole detector amplifier (not in the balance output amplifier BOA-2) active only with larger output swing to avoid over-driving the Main Detectors by gross unbalance of the bridge.

To maintain symmetry of the limiting action there is an adjustable offset zeroing network at the input of the output amplifier.

4.9. The ΔC Meter Amplifier

Diagram 14 - ADC-2 (PC Board No. 2)

The ΔC meter amplifier drives the ΔC meter displaying the capacitance deviation. The integrated amplifier LM 301A is coupled as a unity gain, inverting amplifier and is driven from the ΔC (90^{o}) Main Detector (Board No. 13). Its output is connected directly to the output socket at the rear panel and through a variable resistor to the ΔC meter. The meter should have full scale deflection for a one volt output and the series resistor is made variable in order to compensate for meter coil resistance variations. Another potentiometer controls the offset of the amplifier to secure a zero output for zero input.

On the same PC Board is placed a dual-in-line reed relay controlled by the %/pF switch on the bridge unit. It shorts to earth the X (ΔC) input of the adjoining multiplier in the pF deviation mode.

4.10. The Multiplier

Diagram 15 - MUL-2 (PC Board No. 4)

The multiplier employs the monolithic multiplier circuit SG 1595L in conjunction with two operational amplifiers. These form a feed-back loop from the current output pins 2 and 14 to one of the inputs (pin 9). The output to pin 9 also provides the tgδ meter voltage which is limited by diodes to ground.

The tgδ Main Detector output is applied in opposition to the multiplier output to the input of the second operational amplifier. Thus, due to the feed-back circuit, the multiplier output between pins 2 and 14 will be proportional to the tgδ detector output.

For a given value of tgδ the detector output is proportional to (1 + ΔC).

By varying the multiplier gain in the same proportion the input voltage at pin 9 and the meter voltage are kept constant for variations in ΔC.

The gain variation is achieved by applying the 0^{o} Balance Detector output (±10 volt proportional to ΔC) to the gain controlling input at pin 4. This input is biased by a negative voltage on pin 8 to give correct gain variation with ΔC.

To obtain correct adjustment of the circuit 4 pre-set multiturn potentiometers are provided.

RV1 sets gain variation with ΔC and is adjusted to give constant meter reading for a fixed $tg\delta$ and varying ΔC values from -60% to +60%.

RV4 sets the correct meter deflection corresponding to the $tg\delta$ detector input.

RV2 corrects multiplier offset and is set at +60% ΔC to adjust meter zero.

RV4 corrects operational amplifier offset and is set at -60% ΔC for meter zero.

4.11. The Bridge Module

Diagram 19

Physically, this falls into three sections:

1. A shielding box containing the standard capacitor and the various correcting capacitors.

2. A printed circuit board carrying the ratio transformers, range and mode switches and the circuit for setting of $tg\delta$ and zero capacitance.

3. The front panel with the measuring terminals and the four-terminal compensating circuit.

The separate circuits are described in detail in the following paragraphs.

1. Standard Capacitor Circuit

The standard capacitor consists of two decades 10x20pF and 10x2pF. Each decade is made up of 4 capacitors with the values 1, 2, 3, and 4 units, which are switched in parallel as required. The capacitors are switched either to the generator or to ground to eliminate stray capacitance errors and to achieve constant impedance - regardless of setting - at the detector junction. This is essential for the correct operation of the four-terminal circuit described later.

A calibrated differential capacitor is provided for fine adjustment.

A pre-set trimmer capacitor N_o connected to a voltage opposite in phase, to that of the standard, neutralizes the standard's zero capacitance.

To compensate varying zero capacitance at the measuring terminals, a 10-turn variable capacitor C_o (10pF) is provided. This is fed by a voltage half the value of the measuring voltage and of opposite phase, so that up to 5pF

zero capacitance may be compensated. This capacitor is adjustable from the front panel ("C_o").

Two phase shifting circuits are included for compensating residual quadrature errors at zero setting for the two lower ranges. Each consists of a 300kΩ resistor mounted in a grounded metal tube.

An adjustable voltage in phase with the measuring voltage is applied to one terminal of the resistors while the other terminal is coupled to the detector point by a small capacitance. The distributed stray capacitance to the metal tube provides a 90^o phase shift.

The coupling capacitor (20pF) for injecting the balancing voltage in the pF/Gp mode is also mounted in the standard section.

2. Printed Circuit Board

2.1. Range x0.1

The bridge ratio transformer (L1) provides a 2 to 1 ratio between the measuring voltage (V_x) and the standard voltage (V_N). The low end of the V_N winding is connected to the mode switch and is switched either to the balancing input (BAL) or to ground through an L-R network which simulates the impedance of the BALANCE cable.

The Reference Voltage is taken from a tap on the V_x winding at 1/10 of the total winding.

A phase-correcting circuit adjusted by the pre-set potentiometer "tgδ/ΔC x0.1" places the reference exactly in phase with the V_x voltage.

The V_x and V_N voltages must be of exactly opposite phase. This is set by a pre-set potentiometer "tgδ x0.1" and a series resistor connected across the V_N winding.

The standard capacitor C_N is adjusted for correct capacitance reading on the x1 range.

Any small ratio errors on the x0.1 range are corrected by connecting a capacitor of an appropriate value across the V_x winding.

To neutralize the zero capacitance across the measuring terminals a winding in ratio 1:2 to the V_x winding giving a voltage V_o of opposite phase to V_x is switched to the zero adjust capacitor "C_o" in the N box.

A pre-set potentiomer "tgδ_o x0.1" is connected between the V_x output and the above V_o output to supply the phase shifter in the N box described previously. This potentiometer corrects the tgδ offset at zero capacitance setting.

2.2. Range x1

On this range the transformer L2 is switched in. This has a ratio of 5 to 1 between V_N and V_x. The low end of the V_N winding is connected to the mode switch along with the corresponding x0.1 winding.

The Reference Voltage is taken directly from the V_x output. Small corrections to the transformer ratio are again achieved by fixed capacitors across the V_x winding.

Phase correction is made by the pre-set potentiometer "tgδ x1" in series with a fixed resistor. A resistor in series with the V_N winding brings the correction within the adjustment range of the potentiometer.

For C_o correction, a winding of opposite phase to the V_x winding is switched in ($V_{o(1)}$).

As on the x0.1 range a pre-set potentiometer "tgδ_o x1" is provided, connected to a second phase shifter on the standard box.

This corrects the tgδ offset at zero capacitance on the x1 range.

2.3. Range x10

On this range the x1 transformer L2 is used for supplying the correction voltages to N and the Reference Voltage. A transformer L3 with a tap at 1/10 is switched across the V_x winding of L2 with X connected to the tap.

Phase correction is made by a pre-set potentiometer "tgδ x10", and ratio correction by a fixed capacitor between the tap and the high terminal of L3. C_o correction is applied through a 10 to 1 capacitive divider connected to the V_o winding on L2.

2.4. Bridge Supply and N_o Compensation

The generator output from the main unit is fed to the primary of L5.

The secondary is centre-tapped for the x1 and x10 range.

The whole secondary is used for the x0.1 range. The supply voltage from L5 secondary is connected directly to one of the X terminals and to the N terminal on its box.

The primary of the transformer L4 is connected permanently to the N generator terminal. A winding of ratio 1/3 in opposite phase supplies the adjustable capacitor N_o in the standard box to neutralize the zero capacitance of the standard. A resistor in series with N_o corrects the phase.

2.5. Mode Switching

The two-position push-button mode switch (ΔC %/tgδ - ΔC pF/Gp) connects in its upper position the balance voltage input to the low terminals of the V_N windings of L1 and L2, and thus injects the balance voltage in series with the voltage from the ratio transformers. In this position it connects the 20pF coupling capacitor to ground.

With the switch depressed the balance voltage is switched to the 20pF capacitor coupling it directly to the detector point. The low terminals of the V_N windings are now connected to ground via the L-R network previously mentioned.

A separate contact closure in this switch position activates a relay in the main unit which disables the divider circuit correcting the tgδ meter reading.

3. Front Panel Circuits

The upper terminals (marked 1) are the current terminals. A compensating circuit for four-terminal measurement is mounted in a shielding box beside the detector terminals.

The circuit functions are as follows:

The primary winding of L5 is connected between the lower generator terminal of X and the ratio transformer output. The voltage across this winding is the total error voltage due to all lead impedances on the generator side, including lead impedance and contact resistance at X.

The secondary winding is connected between the lower detector terminal and the detector output. As the detector output is always at zero voltage and L5 is a 1:1 transformer, a voltage equal in amplitude and phase will appear at the detector terminal.

The effective measuring voltage between the two lower sensing terminals is consequently equal to the voltage at the bridge ratio transformer output, irrespective of lead impedance.

The error voltage at the lower detector terminal added to the voltage due to impedance in the current lead to the upper detector terminal from the standard will cause an error in the voltage across the standard. As the capacitance of the standard seen from the detector is constant - about 400pF - for all settings, this error may be compensated by applying a voltage equal to the error voltage to a capacitor equal to the capacitance of the standard and connected to the detector output.

In the circuit an emitter follower with the base coupled to the upper detector terminal drives the correcting capacitor. A phase shifting circuit adjusted by a pre-set trim-cap. ensures correct phase, and the capacitance is adjusted by padding with fixed capacitors.

The compensating circuits reduce errors by a factor of about 30, compared to two terminal measurements.

A phase-shifting circuit, incorporating the front panel potentiometer Gp_o, feeds a current into the detector output in the correct phase to compensate any parallel conductance in the test fixture.

4.12. The Power Supply

Diagram 20

The regulators for the power supply voltages (±15V, +12V, and -8V) are placed together in a printed circuit board mounted on the rear panel of the Main Frame together with the power transformer, the line voltage selector, the fuse and the line voltage input socket.

The ±15V supply is designed with an integrated dual-voltage regulator driving two power transistors (2N3055) mounted on heatsinks. Two potentiometers control the output voltage values and balance respectively.

The +12V and -8V supplies are independent and similar.

They are designed with the integrated regulator μA723 driving a 2N3055 output transistor.

Potentiometers for precise output voltage setting are provided.

5. MAINTENANCE

Diagrams 16, 17, and 18

The adjustments by the front panel controls - as described in the Operating Instructions - should suffice for a trouble-free long term use. In case of repair being made or if a degrading of the measuring accuracy appears which cannot be countered by the front panel adjustments, a realignment of the factory-set potentiometers and trim-caps. inside the apparatus may be necessary.

The user is warned to follow the instruction manual and not touch the controls marked in Diagram 17 with a broken line. These controls cannot be adjusted without special measuring aids.

If the CDB 1 develops a serious fault or if a full readjustment is called for then the apparatus should be returned to the factory for repair.

If an adjustment is attempted it is necessary to use a digital voltmeter (DVM), an amplifying AC-voltmeter (AVM), a counter and an oscilloscope with a high impedance probe.

The following procedure is divided in two parts: first an alignment of the electronics frame alone and second the alignment of the whole system.

5.1. Alignment of the Main Frame

Remove the top cover and disconnect the bridge unit. Short the GEN. and REF. terminals with a coax cable and BNC T adapter and connect another coax cable to the adapter. The short between the GEN. and REF. terminals should remain on for the whole readjustment of the Main Frame. Allow for heat-up period before any measurements are made.

Some of the following measurements are best made on the underside of the interconnection circuit board.

Place the frame on its side and remove the bottom cover. Check first the four power supply voltages -8V, +12V, +15V, and -15V (pins 6, 13, 19, and 20 counted from the front side on the edge connectors in both rows) with the DVM. They are adjustable with the single-turn potentiometers on the supply board mounted on the rear panel. They should no deviate more than a few millivolts from the nominal values.

Note: Most detectors have a piece of wire protruding from the component side of the boards, connected to the DC output as a test point. This gives easy access to measure the output from the topside of the main frame.

5.1.1. Adjustment of the Generating System

This system consists of the Oscillator (OSC-2, Board No. 1), the Amplitude Detector (ODA-2, Board No. 3), and the Reference Input Amplifier (AAC-2, Board No. 5) now connected together in a loop with the short between the GEN. and REF. terminals.

Connect the coax cable from the short point to the AVM and adjust the Oscillator's output amplitude to 0.300V RMS with the amplitude control potentiometer on the Amplitude Detector (ODA-2, see diagram 17).

The front panel potentiometer "ΔC 20% ADJ." is another amplitude control for fine adjust, connected directly to the oscillator. It should be set to approx. +5V on its center pin before the amplitude adjustment with the ODA-2 potentiomter.

Connect the short point (between GEN. and REF. terminals) to the counter and adjust the frequency to 1.000MHz with the frequency control trim-cap. on the oscillator board OSC-2.

5.1.2. Adjustment of the 90^{o} Reference System

This system consists of the 90^{o} Phase Correction Generator (AGE-2, Board No. 7), the 90^{o} Squaring Amplifier (SQT-2, Board No. 9), and the 90^{o} Phase Control Detector (PDT-2, Board No. 11) looped together. Observe with the oscilloscope the squarewave references (90^{o} and 270^{o}) on pins 8 and 9 on the SQT-2 edge connector (9).

Adjust the amplitude to approx. 250mVp-p with the amplitude control potentiometer (single-turn) on SQT-2.

Use an oscilloscope probe or terminate the oscilloscope cable with its characteristic impedance. Otherwise severe ringing owing to the very short rise- and falltimes will disturb the oscilloscope trace.

The squarewaves should appear with very short rise-and falltimes (<10nS) and a 50% duty cycle. Precise duty cycle setting is only possible with special equipment.

Connect the DVM to the output of the Phase Detector PDT-2 (11) (pin 18 on edge connector or the board test point). Adjust the Phase

Detector output voltage to zero with the zero off-set potentiometer (multiturn) on the Phase Correction Generator AGE-2 (7). The three controls on the Phase Detector should not be touched.

5.1.3. Adjustment of 0^{o} Reference System

This system consists of the 0^{o} Phase Correction Generator (GEA-2, Board No. 6), the 0^{o} Squaring Amplifier (SQO-2, Board No. 8), and the 0^{o} Phase Control Detector (PDO-2, Board No. 10) looped together.

For adjustment use the same procedure as under 5.1.1. on the corresponding circuit boards.

5.1.4. Adjustment of the 90^{o} Balance Loop

Remove the Detector Input Amplifier (DAA-2, Board No. 19) and short its output pin to earth (pins 16/17 to e.g. 21/22 on the edge connector (19)).

Remove the 0^{o} Balance Generator (BGO-2, Board No. 18).

Connect the DVM to 0^{o} Balance Detector's output (DBC-2, Board No. 14 - pin 18 or test point on the board).

Off-set the 0^{o} (tgδ) Main Detector's output (MDT-2, Board No. 12) to full scale deviation on the tgδ meter with the zero off-set multiturn potentiometer on the MDT-2 board.

Observe the DVM reading when changing the tgδ range selector between 0.3% and 10%.

Adjust the phase control trim-cap. on the Balance Output Amplifier (BOA-2, Board No. 17) to same reading on both tgδ ranges.

After adjustment reset the MDT-2 Main Detector to zero.

5.1.5. Adjustment of the 0^{o} Balance Loop

This adjustment should only be done after the adjustment described in point 5.1.4.

Reinsert the BGO-2 and remove the 90^{o} Balance Generator (DBT-2, Board No. 16).

Connect the DVM to the 90^{o} Balance Detector's output (DBT-2, Board No. 15 - pin 18 or test point on the board).

Off-set the 90^{o} (ΔC) Main Detector's output (MDC-2, Board No. 13) to negative full scale reading on the ΔC meter with the zero off-set multiturn potentiometer on the MDC-2 board.

Observe the DVM reading when changing the ΔC range selector between 2% and 20%.

Adjust the phase control single-turn potentiometer on the 0^{o} Balance Generator BGO-2 (18) to same DVM reading on both ranges.

After adjustment reset the MDC-2 to zero.

Note: The Main Detector's output voltages will not be very stable owing to the large gain of the detectors. If a stable precision laboratory power supply or other means of producing a stable, precisely setable low source-impedance voltage is available, it will be advantageous to the adjustments under point 5.1.4. & 5. to substitute the detectors with such a source by removing the detector boards and applying the source to pin 18.

5.1.6. Zeroing of tgδ System

With all circuit boards in place connect a 100-200pF capacitor between the BAL. and DET. coax terminals.

Adjust the zero off-set multiturn potentiometer on the 90^{o} Balance Detector (DBT-2, Board No. 15) to zero reading on the tgδ meter.

Another control for this is the front panel potentiometer "tgδ ZERO ADJ.".

It should be set to zero volts on its center pin simultaneously.

Adjust the zero off-set multiturn potentiometer on the 0^{o} Balance Detector (DBO-2, Board No. 14) to zero reading on the ΔC meter.

Remove the capacitor between the BAL. and DET. terminals and adjust the zero off-set multiturn potentiometers on the Main Detectors (Boards 12 & 13) to zero reading on the meters.

5.2. Alignment of Bridge Unit & Complete System

Diagrams 17 & 18

This section describes only the adjustments which are possible without the use of accurate standards. Thus adjustment of e.g. the standard capacitor should not be attempted. If errors in the standard or the range ratios are suspected the unit should be returned to the factory for alignment.

The trimmers for adjusting the standard are shown on diagram 18 inside the broken line and should not be touched.

The only standard required is a capacitor of about 100pF with a known tgδ. For this purpose we recommend the chip capacitors type ATC 100 with wire leads from American Technical Ceramics, USA. These capacitors have tgδ values of about 0.5×10^{-4}.

Adjustment of the unit is done in two steps: Zero adjustment and tgδ adjustment.

5.2.1. Zero Adjustment

Diagram 18

Before zero adjustment of the Bridge Unit is carried out the adjustment in section 5.1.6. must be performed.

Remove the bottom panel of the bridge unit to gain access to the adjustment potentiometers, and plug in the axial-lead test fixtures.

Connect the unit to the main frame.

Set as follows:

Standard capacitor dials to zero.

Mode switch to ΔC pF/Gp.

Range multiplier to x0.1

Turn Gp_o adjustment on front panel fully counterclockwise (until clicking is heard).

and select lowest meter ranges on the main frame.

a. Adjust C_o for ΔC meter zero deflection.

b. Adjust $tg\delta_o$ x0.1 potentiomter for tgδ meter reading of +0.3 on the 2μS scale

Adjust Gp_o potentiometer for zero reading.

c. Switch range multiplier to x1.

Adjust $tg\delta_o$ x1 potentiometer for tgδ meter zero deflection.

Repeat point b and c for precise setting.

If ΔC meter is not at zero on x1 multiplier range adjust N_o (accessible through the hole in the standard box - use isolating trim tool) to ΔC meter zero.

Switch to x0.1 on multiplier and readjust C_o.

Repeat N_o adjustment on x1 and C_o on x0.1 until ΔC meter is exactly on zero on both multiplier positions. (The 0-10pF standard capacitor should be exactly on zero throughout these adjustments).

Set Mode Switch to ΔC%/tgδ.

Range multiplier to x1.

Adjust 0-10pF dial for zero ΔC reading.

This adjustment is very critical, as at zero no balance feed-back is obtained. If necessary adjust $tg\delta_o$ x1 potentiometer slightly to bring tgδ meter reading within the lower third of the scale.

Turn the 0-10pF standard capacitor dial slowly to vary ΔC reading between ±2%.

Adjust the Input Phase Setting trim-cap. on the Detector Input Amplifier (DAA-2, Board 19 in Main Frame) to minimum variation of tgδ meter.

Switch mode to ΔC pF/Gp and readjust $tg\delta_o$ x1 potentiometer to zero tgδ.

5.2.2. Tgδ Adjustments

Place a 100pF capacitor with known tgδ in the test fixture and set as follows:

Standard Capacitor to 1x100pF

Mode Switch to ΔC%/tgδ

Range multiplier to x1

ΔC range to 60% and tgδ range to 0.3%.

Vary the ΔC reading out to -50% in steps by turning the x10pF standard capacitor dial. Out to approximately -30% the tgδ meter reading should be constant within 0.005%. Above -30% ΔC the tgδ reading will drop, the maximum error being approx. 0.03%.

Adjust the zero off-set (phase control) multiturn potentiometer on the 90^o Phase Control Detector (PDT-2, Board No. 11 in the Main Frame) so that the tgδ reading is constant out to approx. -30% ΔC. (Another control for this is the front panel potentiometer "Gp/ΔC ADJ.".It should be set to zero volts on its center pin simultaneously).

If more than very small phase adjustments are necessary repeat 5.1.4., 5.1.5, and 5.1.6.

Balance the bridge as before. ΔC range 2%.

Adjust the tgδx1 potentiometer to correct tgδ reading in accordance with the loss of the 100pF capacitor.

Switch range multiplier to x0.1.

Adjust standard capacitor to balance

Adjust tgδx0.1 to correct tgδ reading

Vary the standard capacitor dials to -30% ΔC reading

Adjust the tgδ/ΔC potentiometer in the bridge module to minimum variation in tgδ reading.

Switch range multiplier to xl.

Insert a lnF capacitor in the test fixture

Balance the bridge to zero ΔC

Read exact capacitance value on standard capacitor dials and loss on tgδ meter.

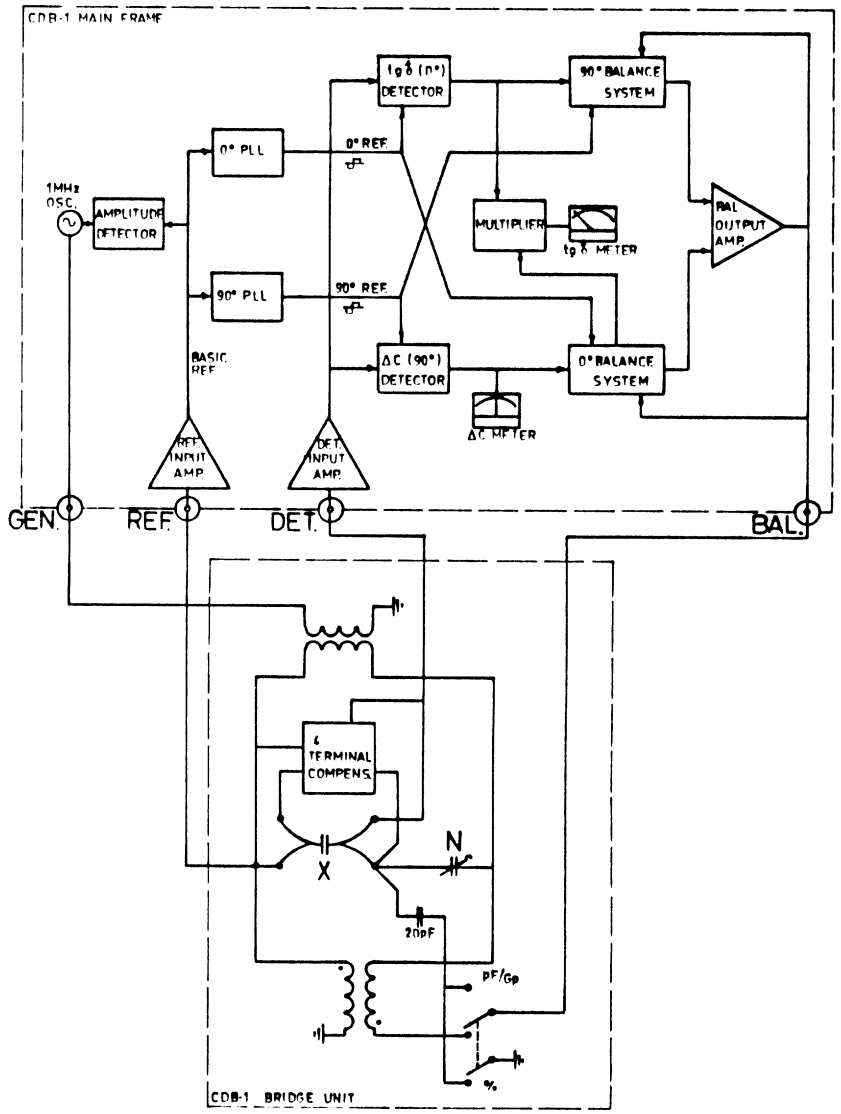
Switch range multiplier to xl0.

Set standard capacitor dials to exactly 1/10 of above setting and check that ΔC meter reading is within 1%

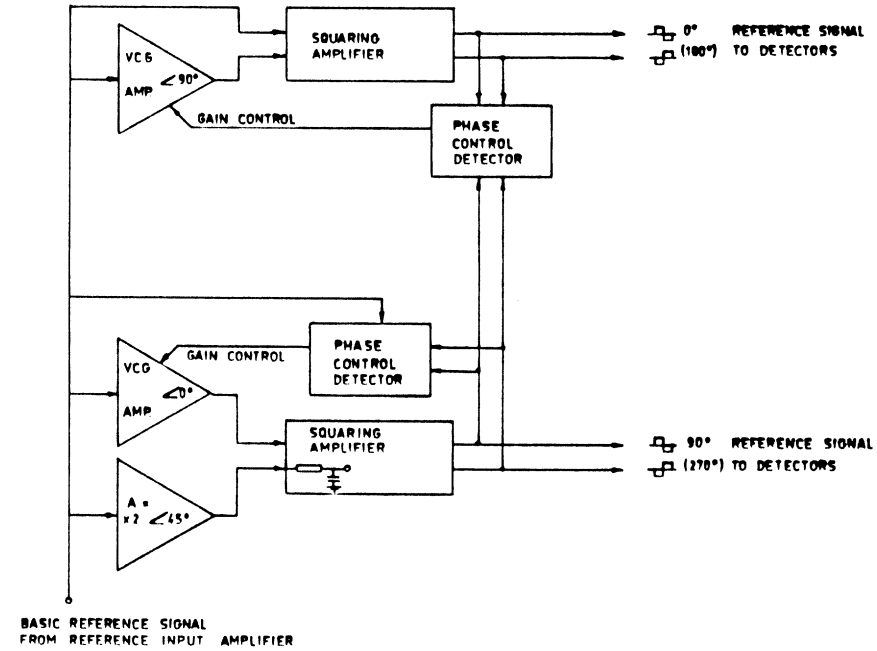
Adjust tgδxl0 potentiometer to obtain a tgδ meter reading equal to that on the xl multiplier range

If the tgδ adjustments made on the three multiplier ranges are more than very small, check the zero adjustments in sections 5.2.1. (including 5.1.6.).

If further zero adjustments are then made repeat section 5.2.2. adjustments.



72360 72361 - 1	CDB1 & B1 DIAGRAM NO. 1 SIMPLIFIED BLOCK-DIAGRAM	RETTET	GODK.
A/S DANBRIDGE		TEGNET 050873 B Rhs KONSTR J.W. HANSEN GODK.	



72360-2	CDB 1 DIAGRAM NO. 2		
A/S DANBRIDGE.	BLOCK DIAGRAM THE REFERENCE SYSTEM	RETTET	GODK.
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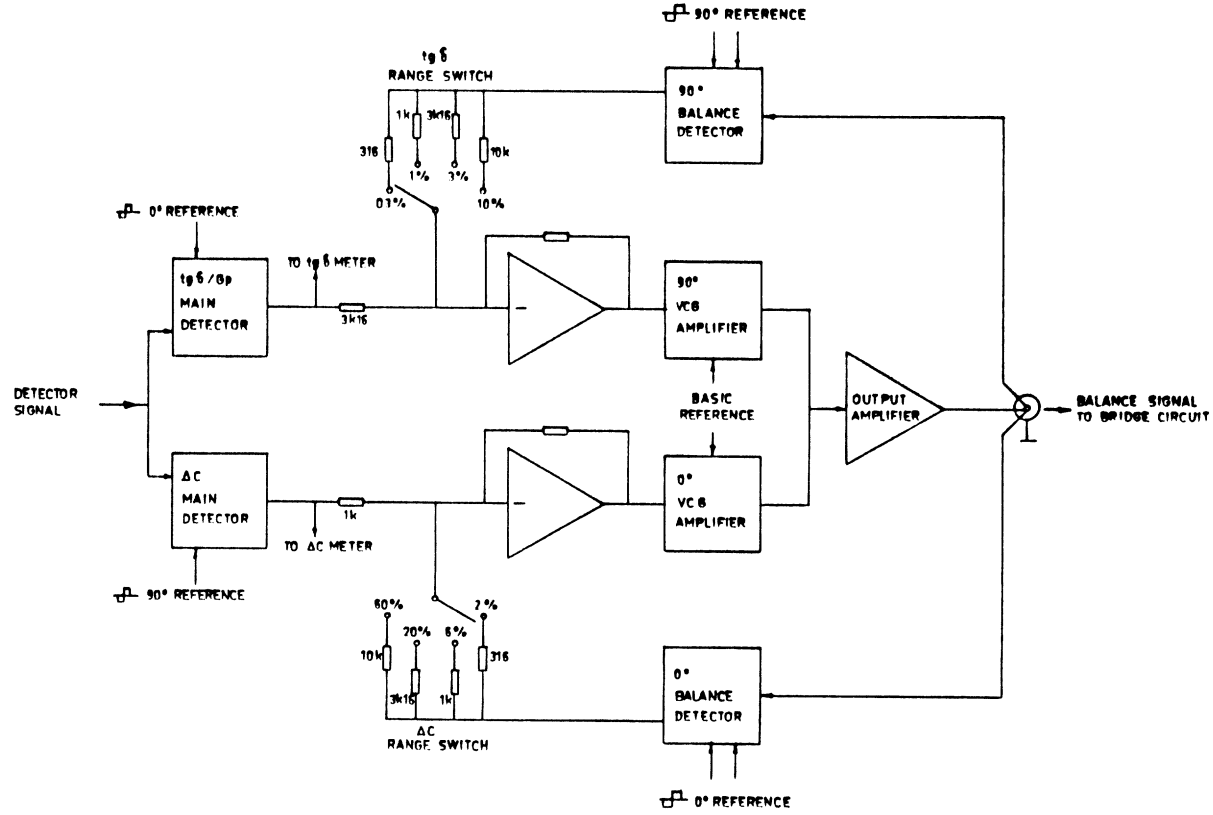
		KONSTR.	J.W. HANSEN
		GODK.	



72360 - 3	CDB1 DIAGRAM NO. 3		
A/S DANBRIDGE.	BLOCK DIAGRAM THE BALANCE SYSTEM	RETTET	GODK.
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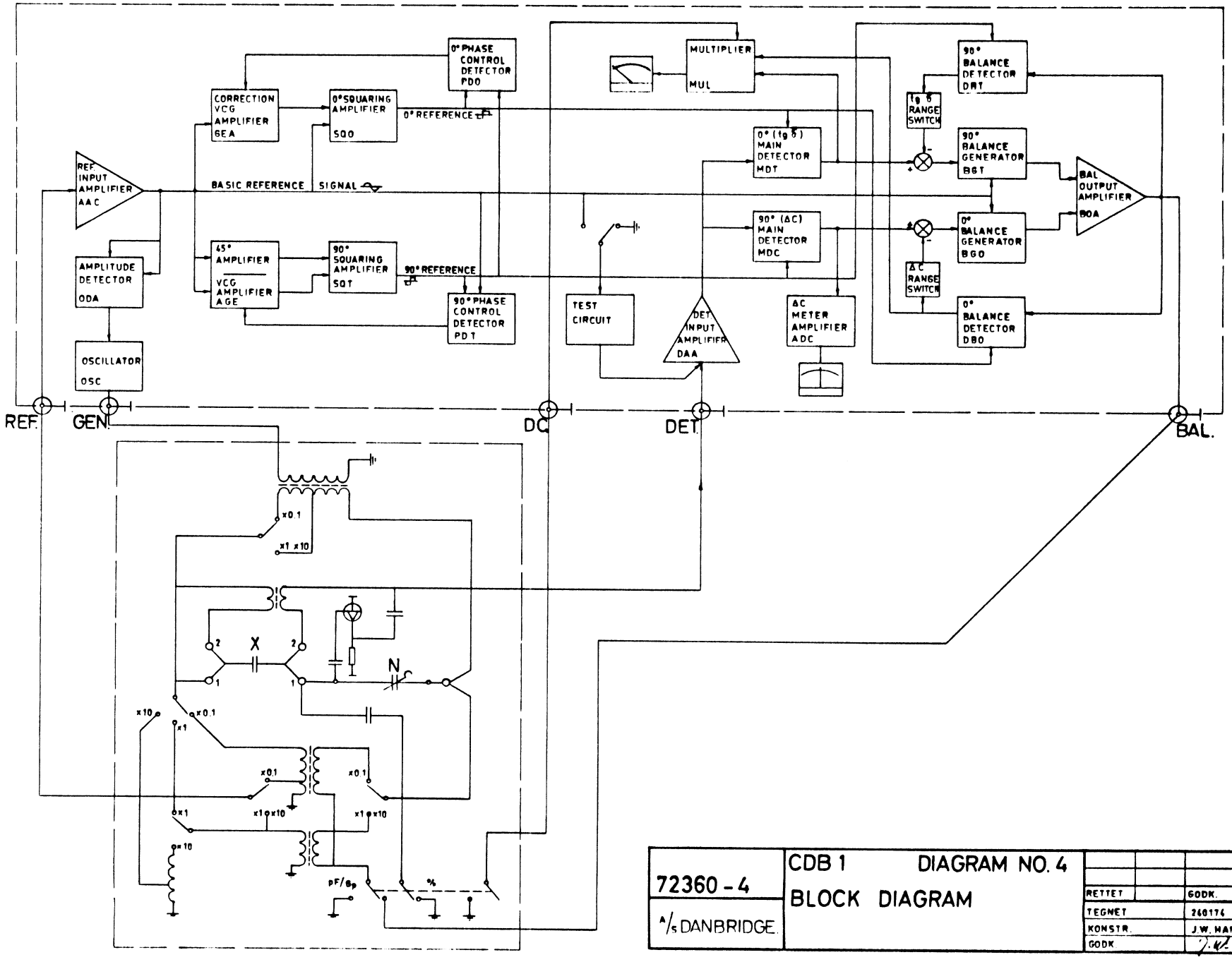
		KONSTR.	J.W. HANSEN
		GODK.	



72360 - 4	CDB 1 DIAGRAM NO. 4		
A/S DANBRIDGE	BLOCK DIAGRAM	RETTET	GODK.
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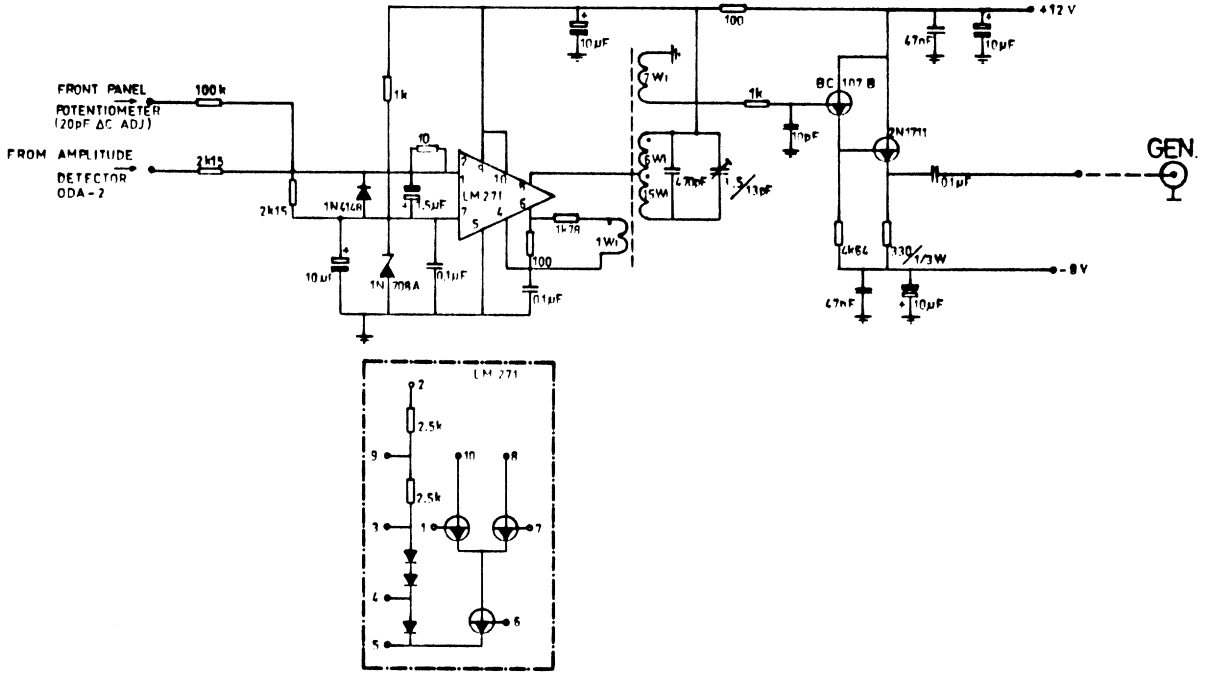
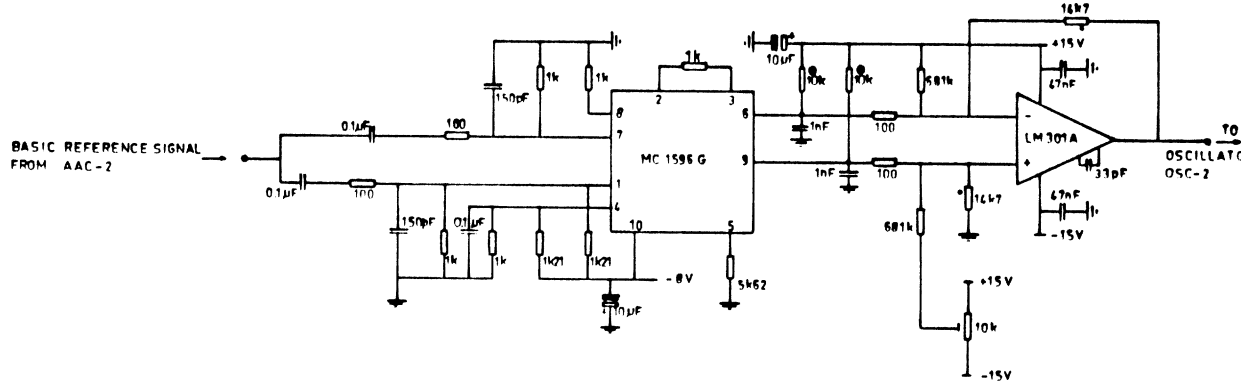
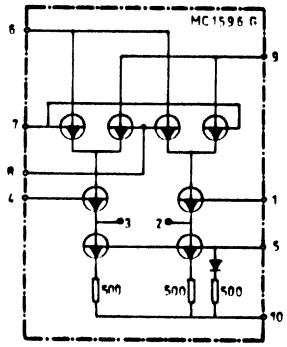
		KONSTR.	J.W. HANSEN.
		GODK	



72360-5	CDB1 DIAGRAM NO. 5 OSCILLATOR	2 300377 BR RETTET	200176 BR GODK.
A/S DANBRIDGE.	OSC-2	TEGNET KONSTR. GODK.	200373 B.Res. J.W. HANSEN





● 0.02 % TC ±5ppM

72360-6	CDB 1 DIAGRAM NO.6		
A/S DANBRIDGE	AMPLITUDE DETECTOR ODA-2		
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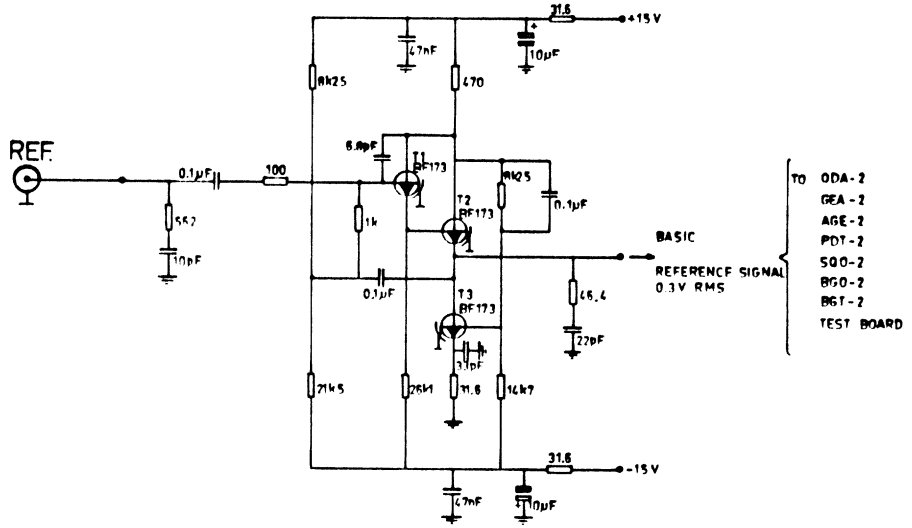
		PETTET 130673 BR	GODK.
		TEGNET	210373 BRas.
		KONSTR.	JW. HANSEN
		GODK.	



72360 - 7	CDB1 DIAGRAM NO.7		
	REFERENCE INPUT AMPLIFIER	RETTET 130873 BR	GODK.
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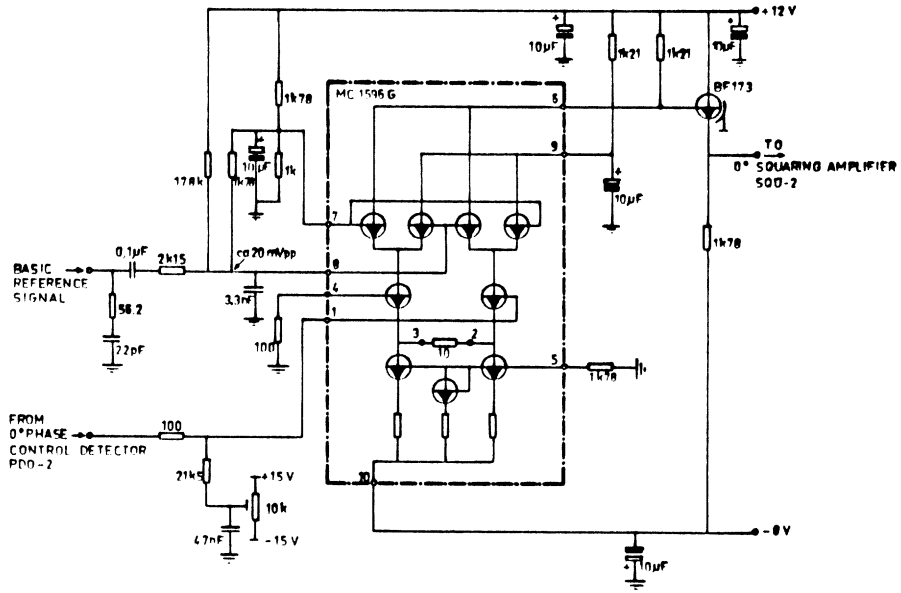
		KONSTR.	J. W. HANSEN
		GODK.	



72360- 8	CDB1 DIAGRAM NO.8		
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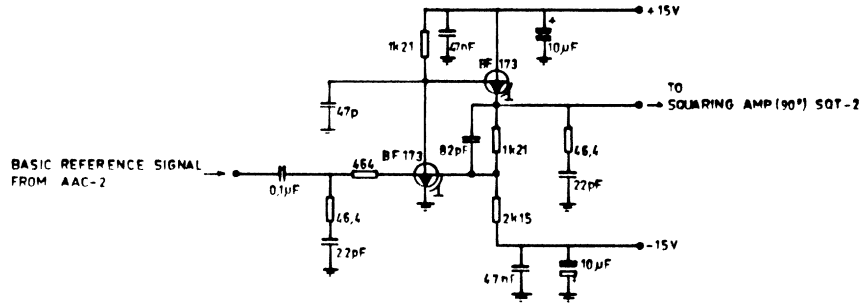
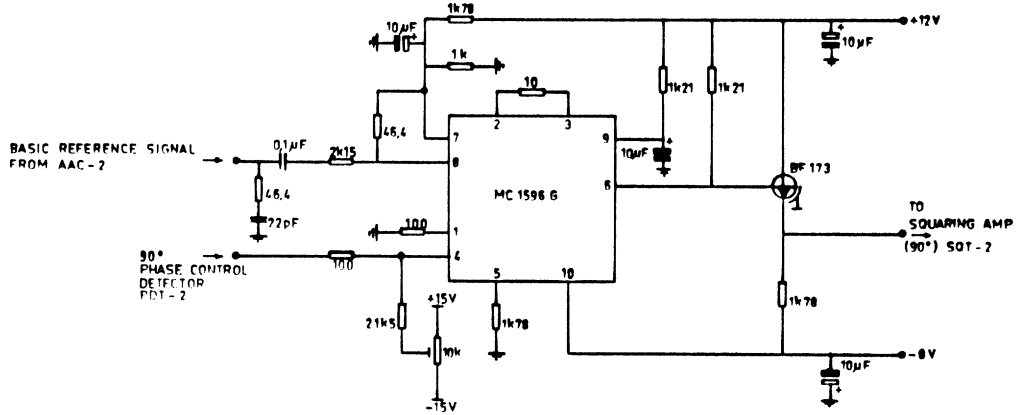
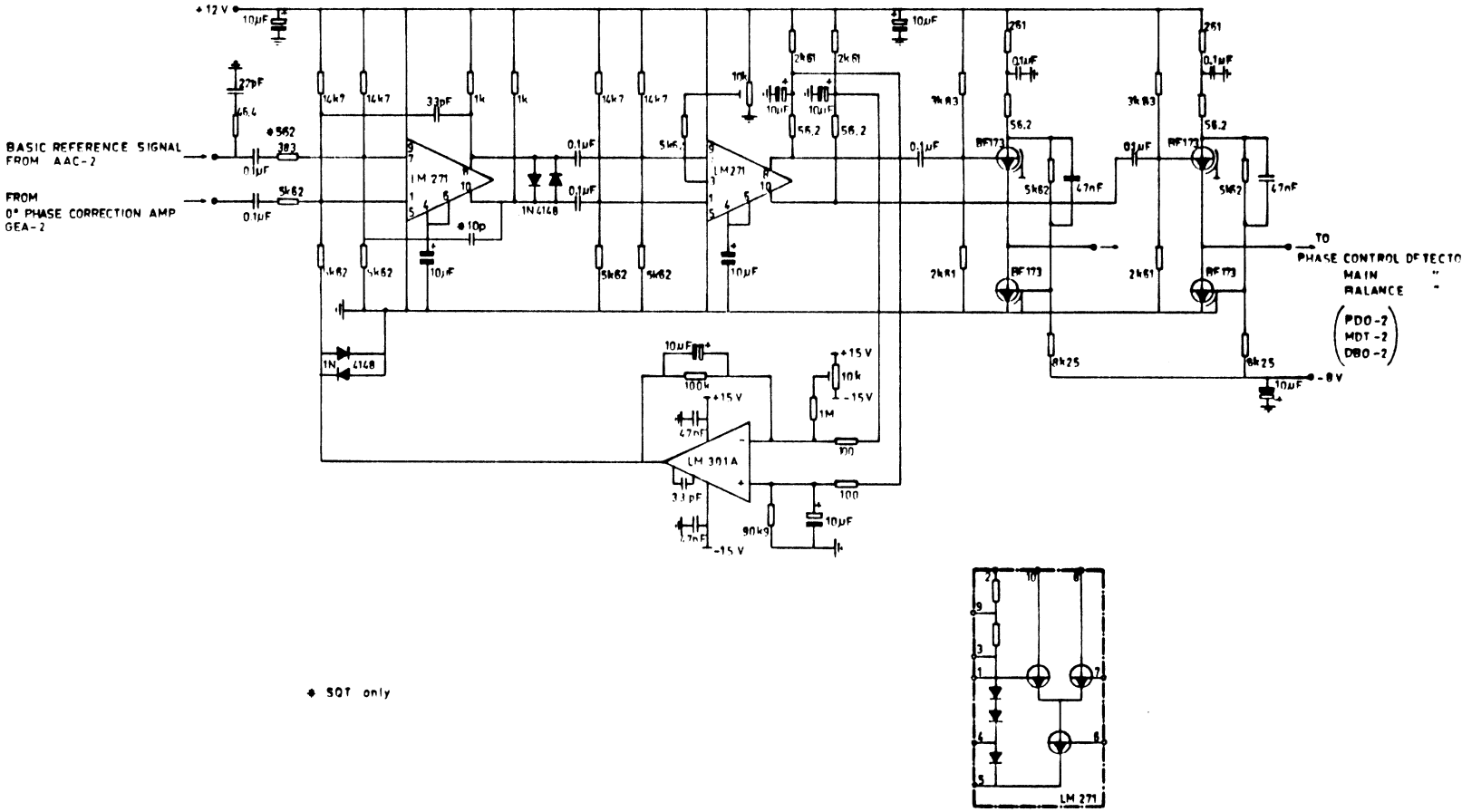
	GEA-2	RETTET 130673 BR	GODK.
		TEGNET	220373 BR
		KONSTR.	J.W. HANSEN
		GODK.	



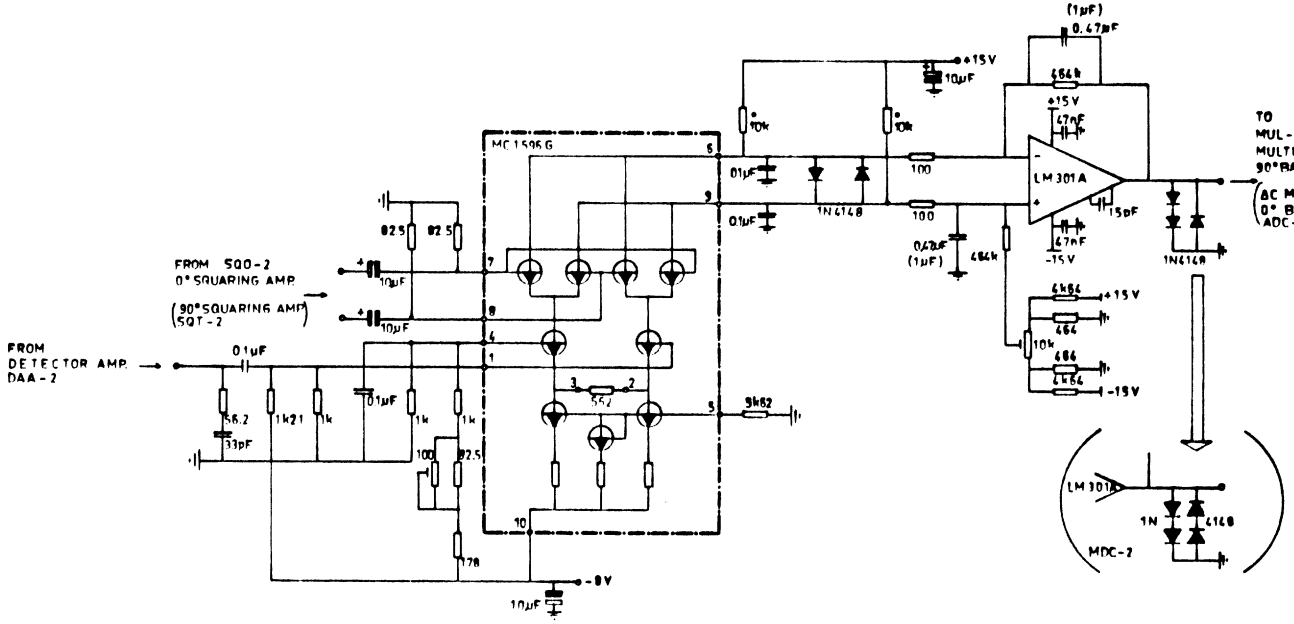


72360-9	CDB 1 DIAGRAM NO. 9		
A/S DANBRIDGE.	45° AMPLIFIER & PHASE CORRECTION AMP.	RETTET 300377BR	GODK.
		TEGNET	120673 B. Ras
		KONSTR.	J.W. HANSEN
		GODK.	



* SQT only

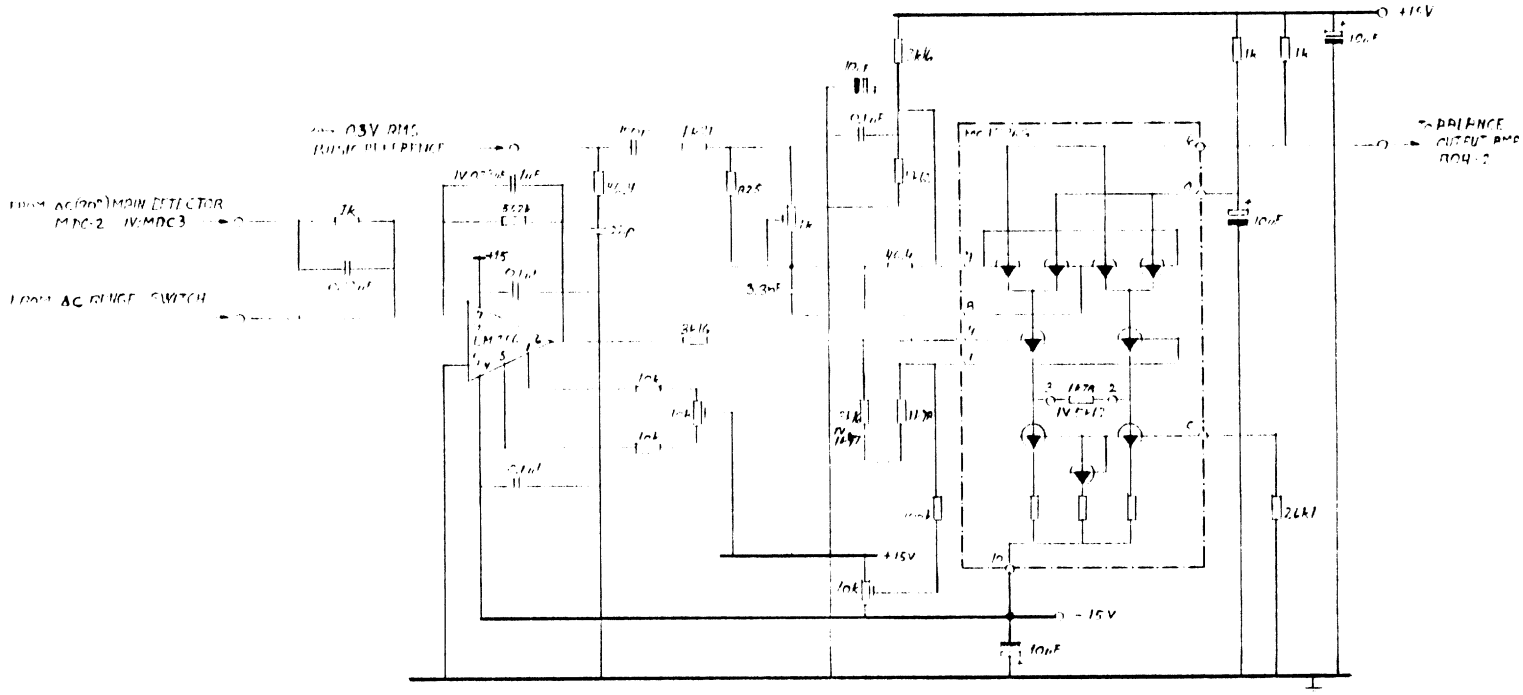
72360-10	CDB1 DIAGRAM NO.10		
A/S DANBRIDGE.	0° SQUARING AMPLIFIER.		
	SQO-2		
		310377BR	
		RETTET 190673 BR	GODK.
		TEGNET	230173 B.Ree
		KONSTR.	J.W. HANSEN
		GODK.	



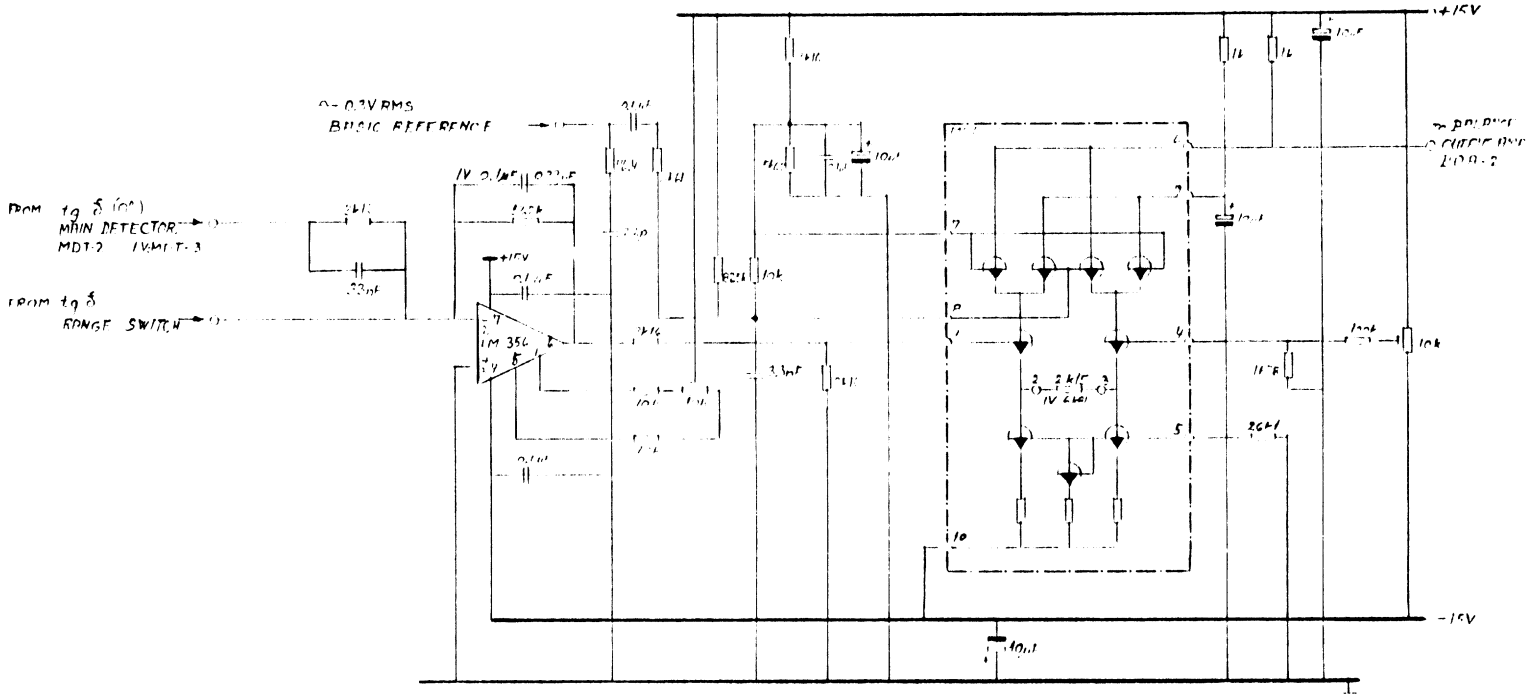
• 0.02% TC ± ppm

72360-11	CDB1 DIAGRAM NO.11	
A/S DANBRIDGE	MAIN DETECTORS 0° & (90°)	
	MDT-2 & MDC-2	

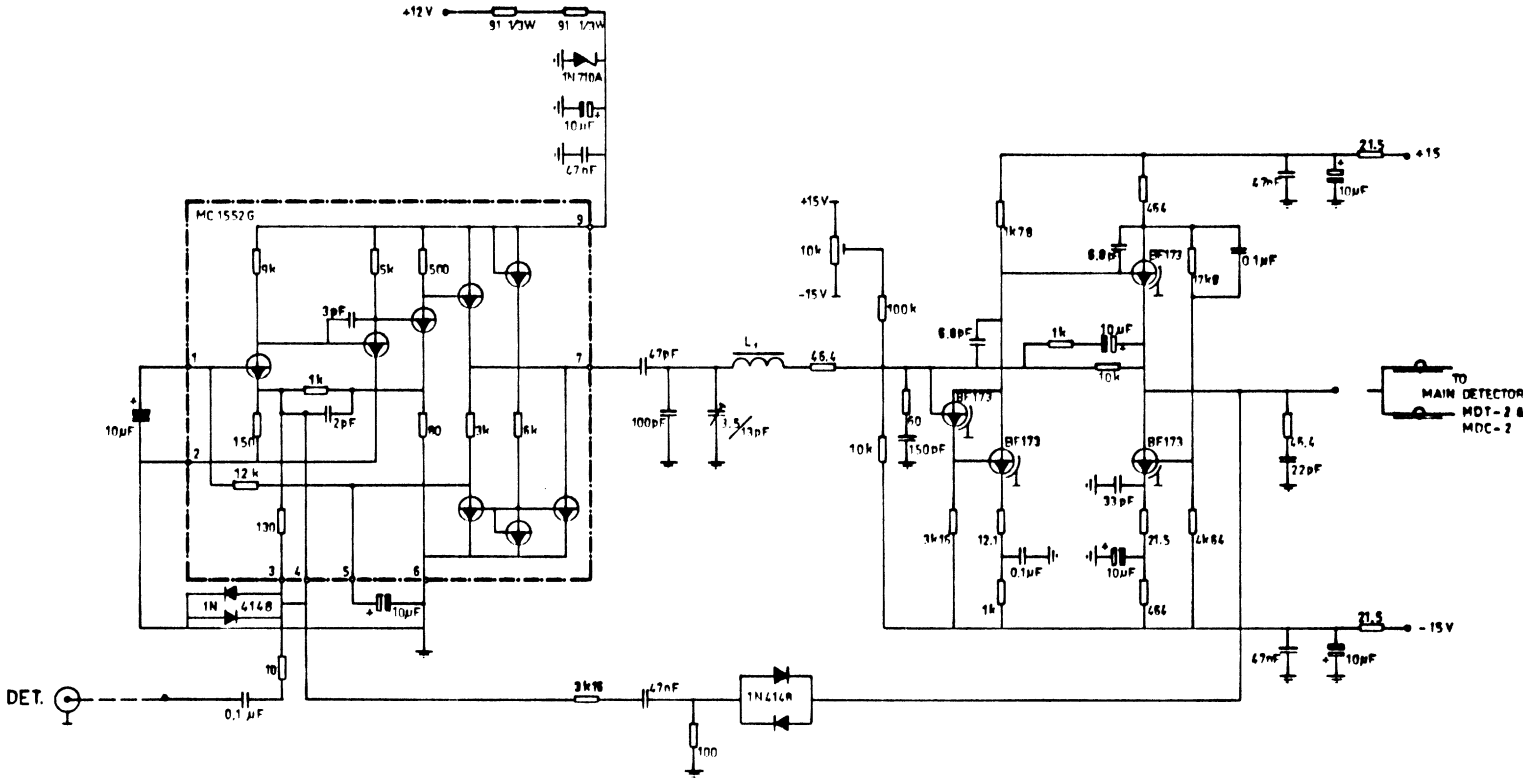
160878 BR	JWH		
RETTET	280178 BR	GODK.	
TEGNET		240373 B Res	
KONSTR.		J.W. HANSEN	
GODK.			



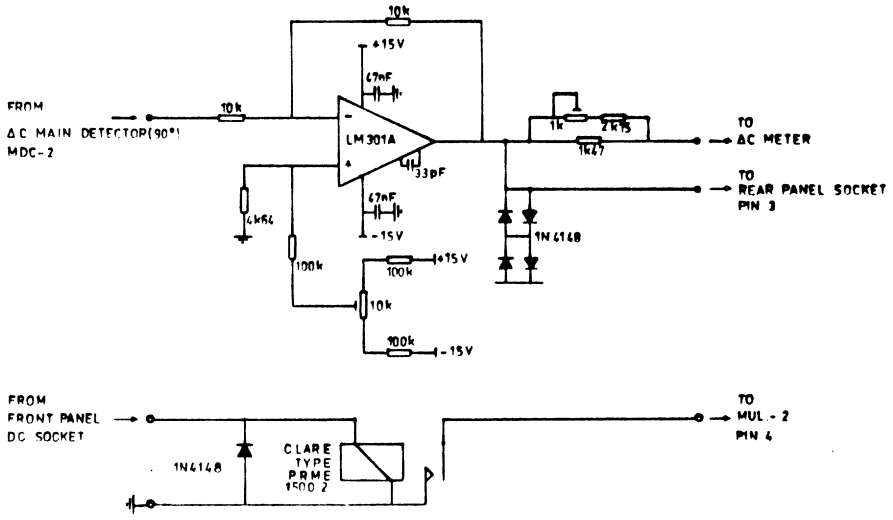
72360-12	CDB1 0.3V AND 1V 0°BALANCE GEN. BGO-3	DIAGRAM NO.12	
danbridge a-s		RETTET / GODK.	
		TEGNET	161080 BRAS
		KONSTRUERET	VAGN JENSEN
		GODK.	



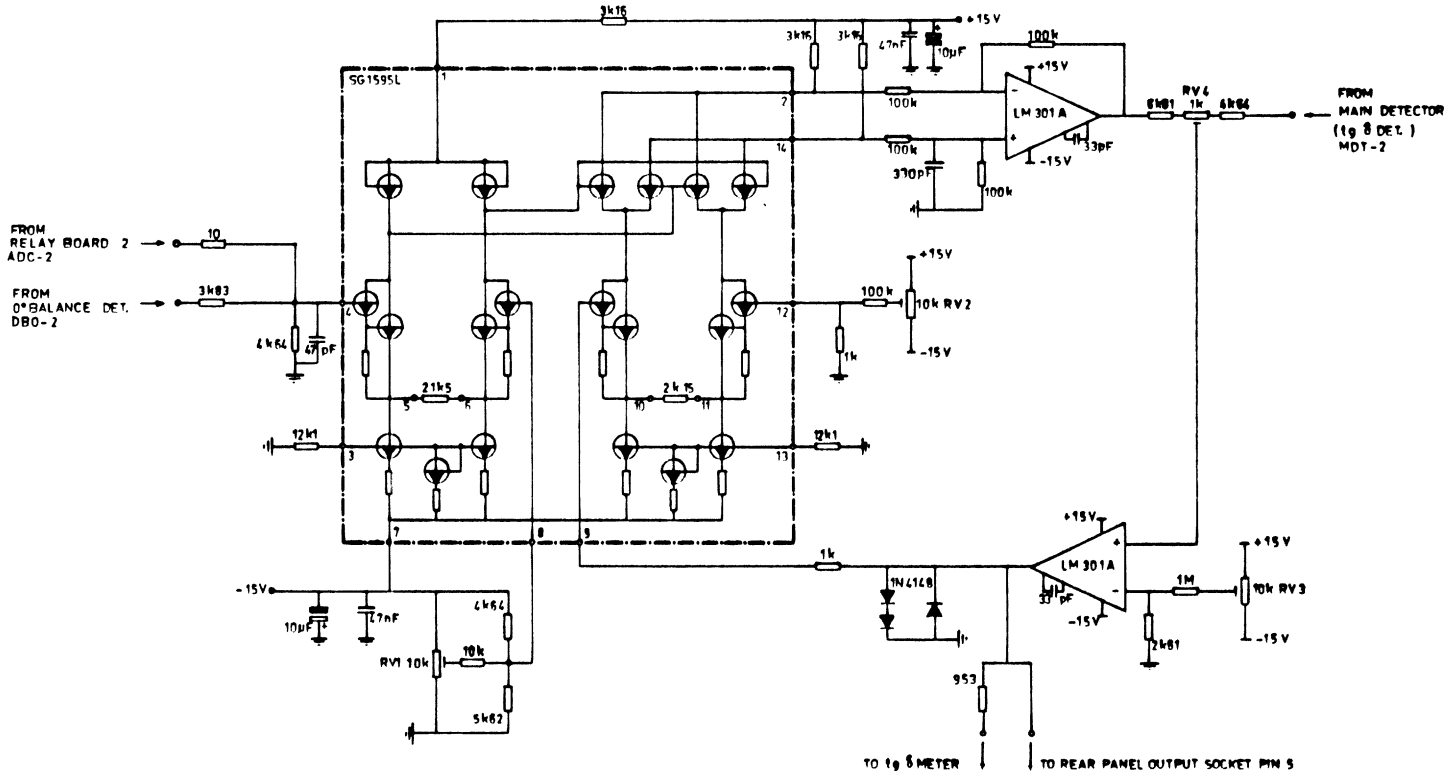
72360-12A	CDB1 0.3V AND 1V 90° BALANCE GEN. BGT-3	DIAGRAM NO.12A	
danbridge a-s		RETTET	GODK.
		TEGNET	231080 BRAS
		KONSTRUERET	VAGN JENSEN
		GODK.	



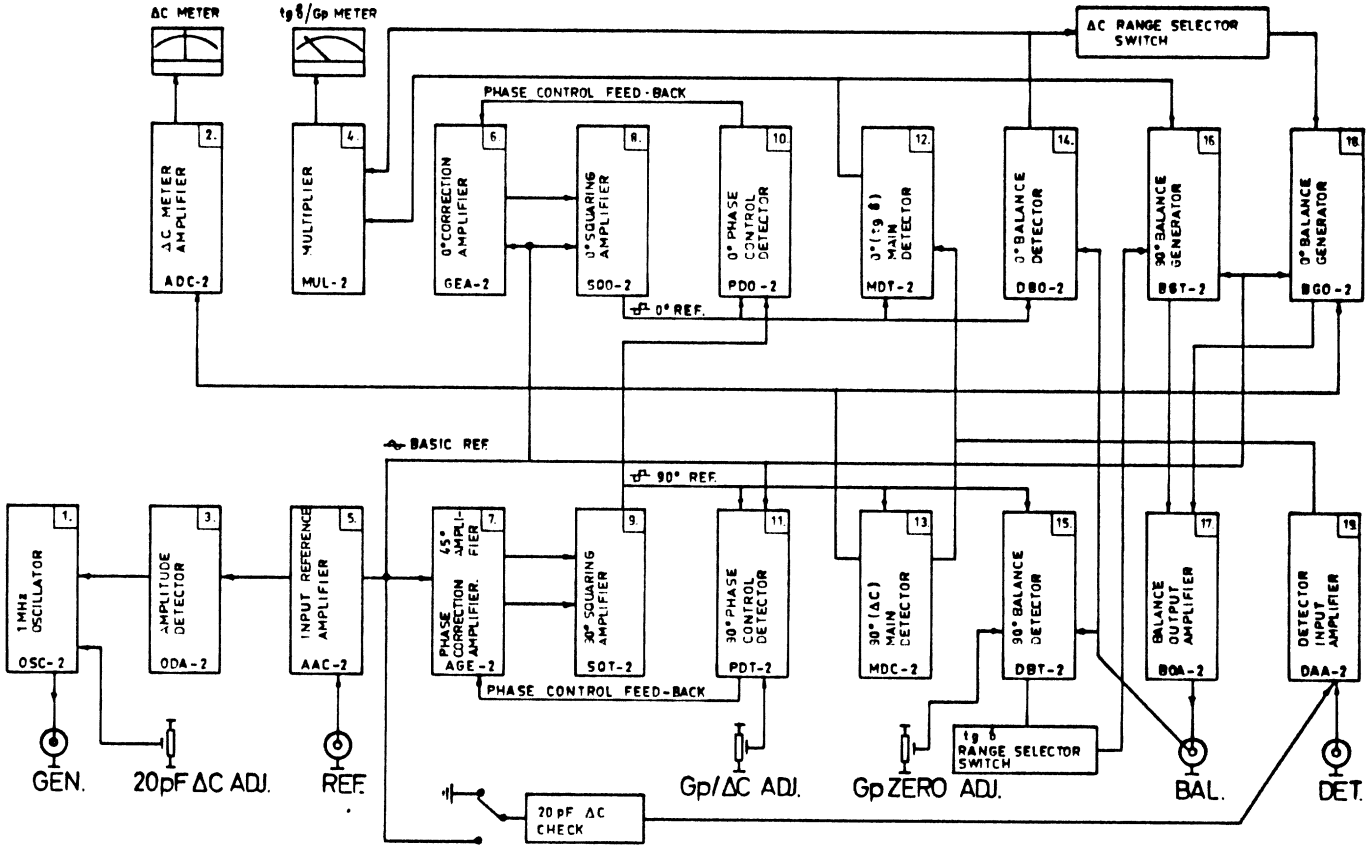
72360-13	CDB1 DIAGRAM NO.13	3003778	
	DETECTOR INPUT AMPLIFIER	RETTET 280176 BR	GODK.
A/S DANBRIDGE	DAA-2	TEGNET	280373 B.Ras.
		KONSTR	J.W. HANSEN
		GODK.	



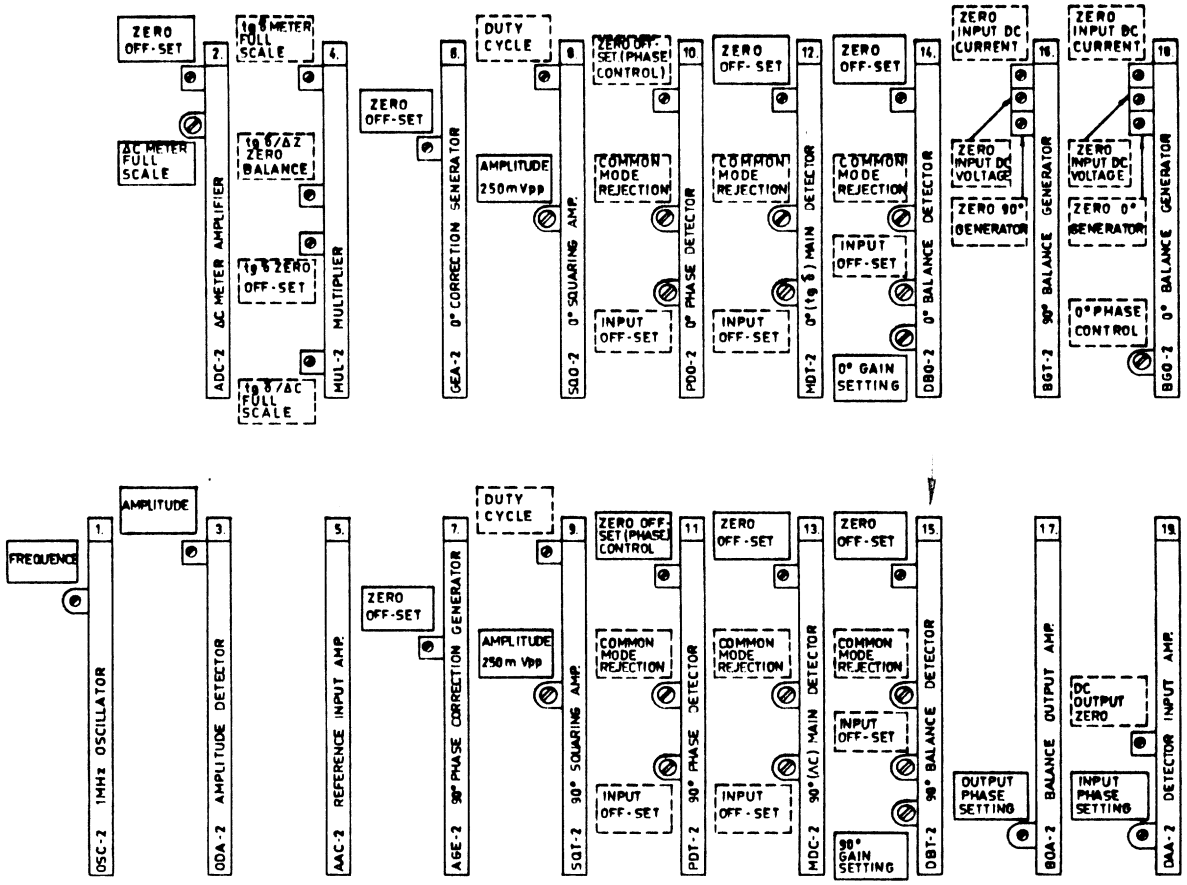
72360-14	CDB 1 DIAGRAM NO.14	
A/S DANBRIDGE	ΔC METER AMPLIFIER	170377 RR RETTET 290176 BR GODK.
	ADC-2	TEGNET 760373 B.Ros
		KONSTR. J.W. HANSEN
		GODK.



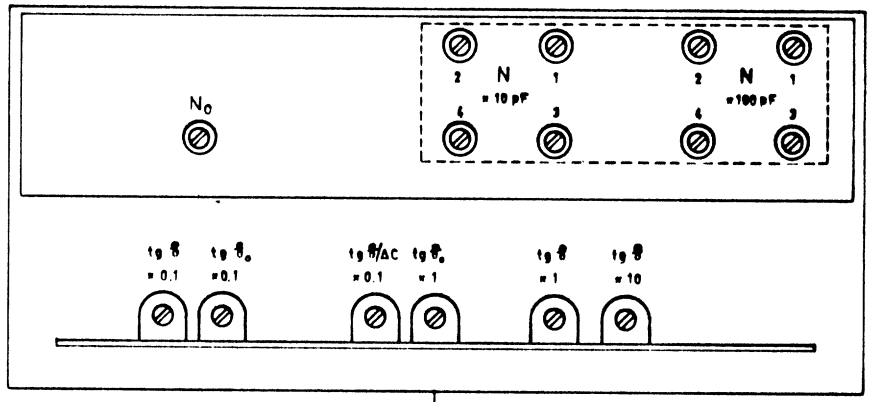
72360-15	CDB1 DIAGRAM NO. 15	310377BR RETTET 300174 BR	GODK. V.V.H
A/S DANBRIDGE.	MULTIPLIER MUL-2	TEGNET MINKTR GODK.	270173 B Ras J.W HANSEN



72360-16	CDB 1 DIAGRAM NO. 16		
A/S DANBRIDGE.	BOARD LOCATION		
		RETTET	GODK.
		TEGNET	120673 B Rns
		KONSTR.	JW HANSEN
		GODK.	

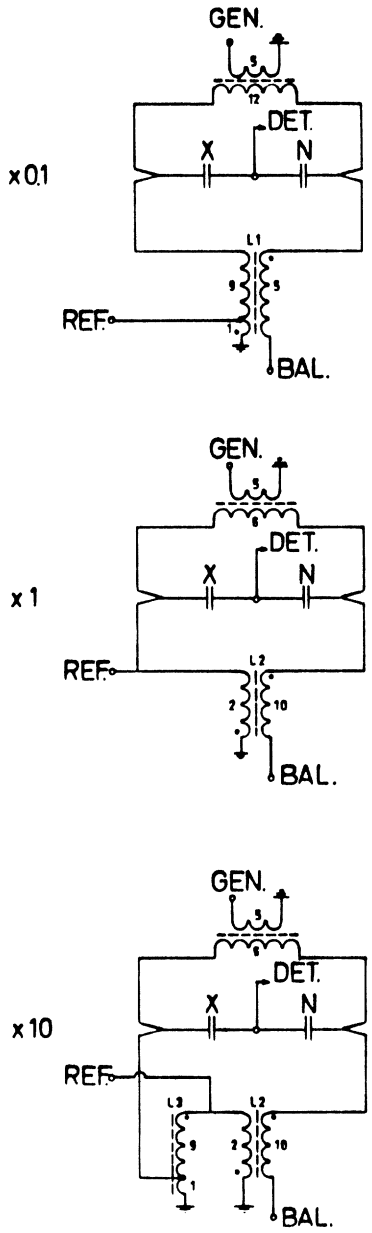


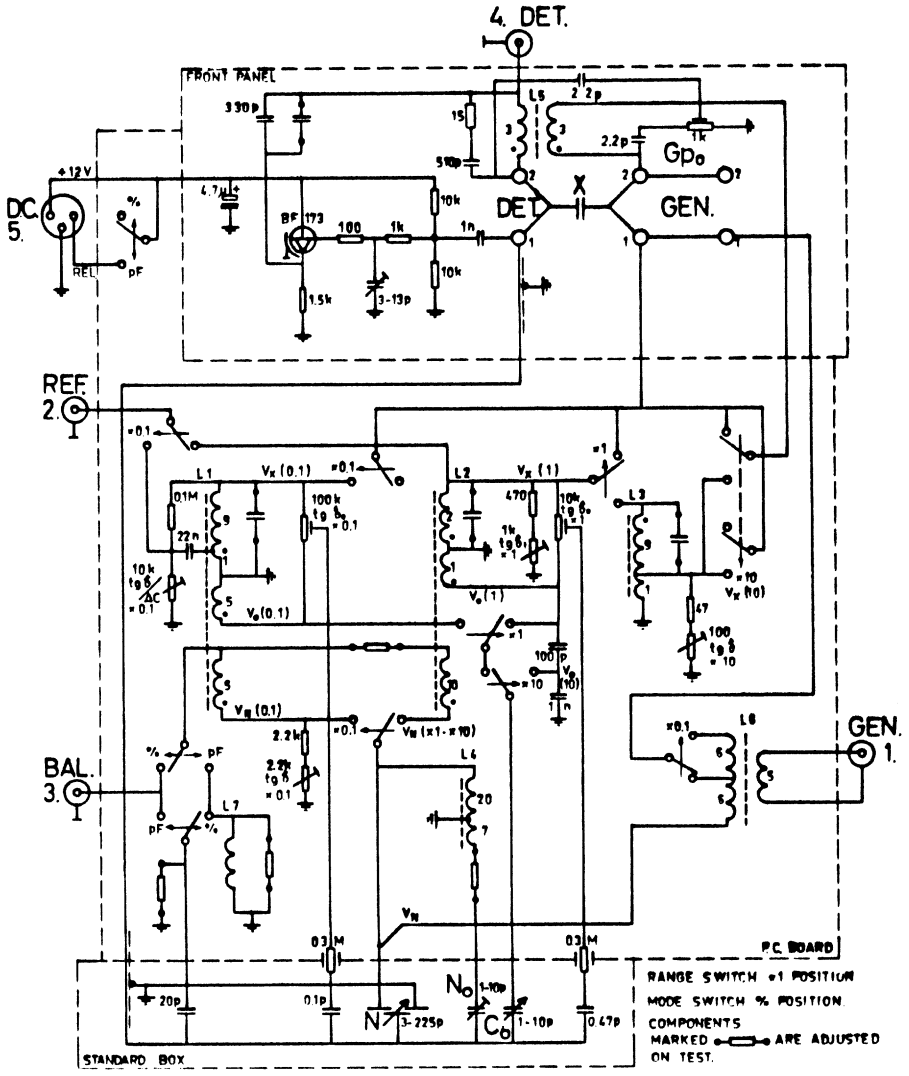
72360 - 17	CDB 1 DIAGRAM NO. 17		
A/S DANBRIDGE	ADJUSTMENTS LOCATIONS	RETTET	GODK.
		TEGNET	280174 B.Rø.
		KONSTR.	J.W. HANSEN
		GODK	



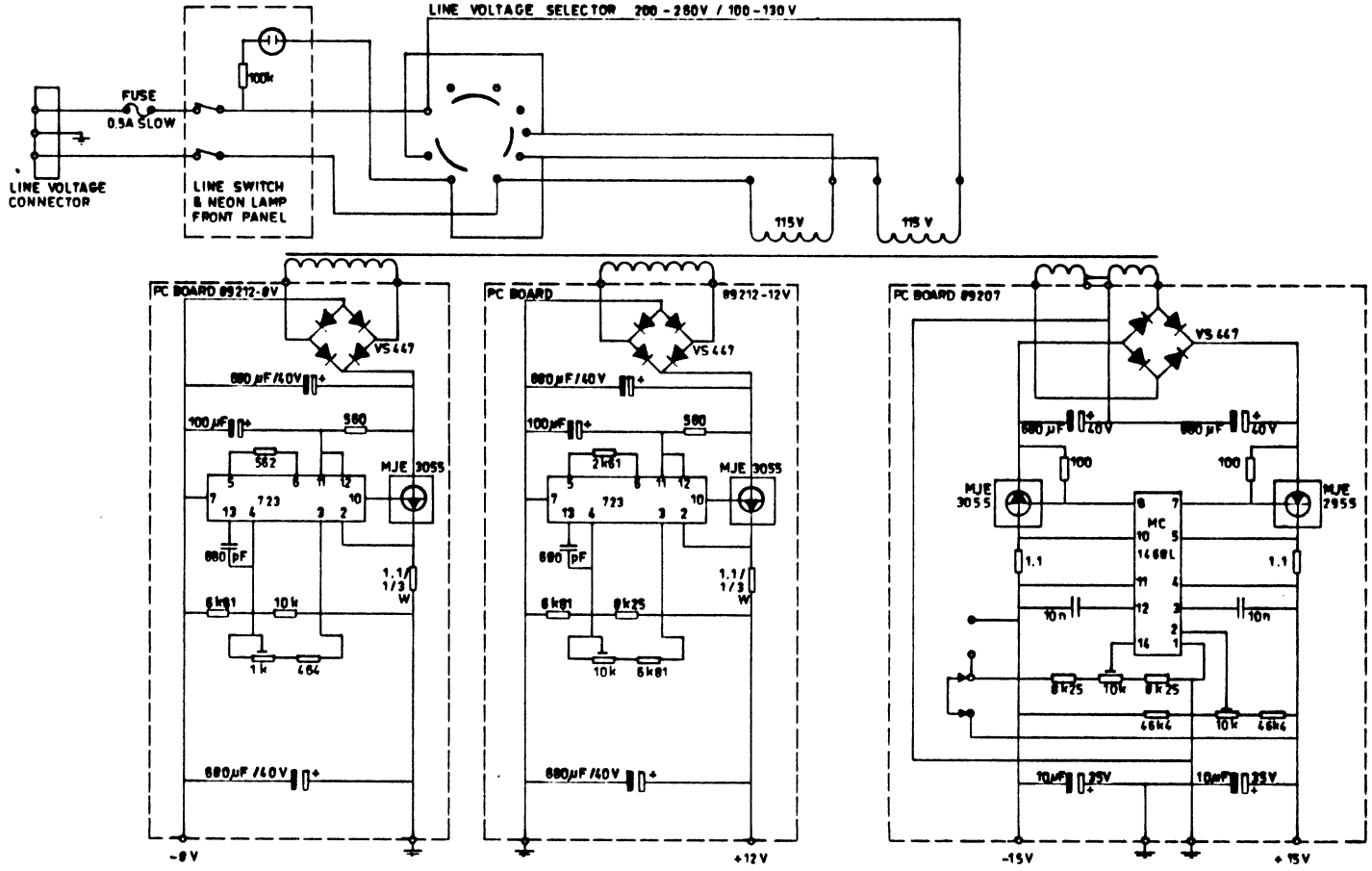
LOCATION OF TRIMMERS
SEEN FROM BOTTOM.

72361 -18	CDB 1-B1 DIAGRAM NO. 18			
A/S DANBRIDGE	BRIDGE UNIT	RETTET		GODK.
		TEGNET		210176 B Ros
		KONSTR.		VAGN JENSEN
		GODK.		



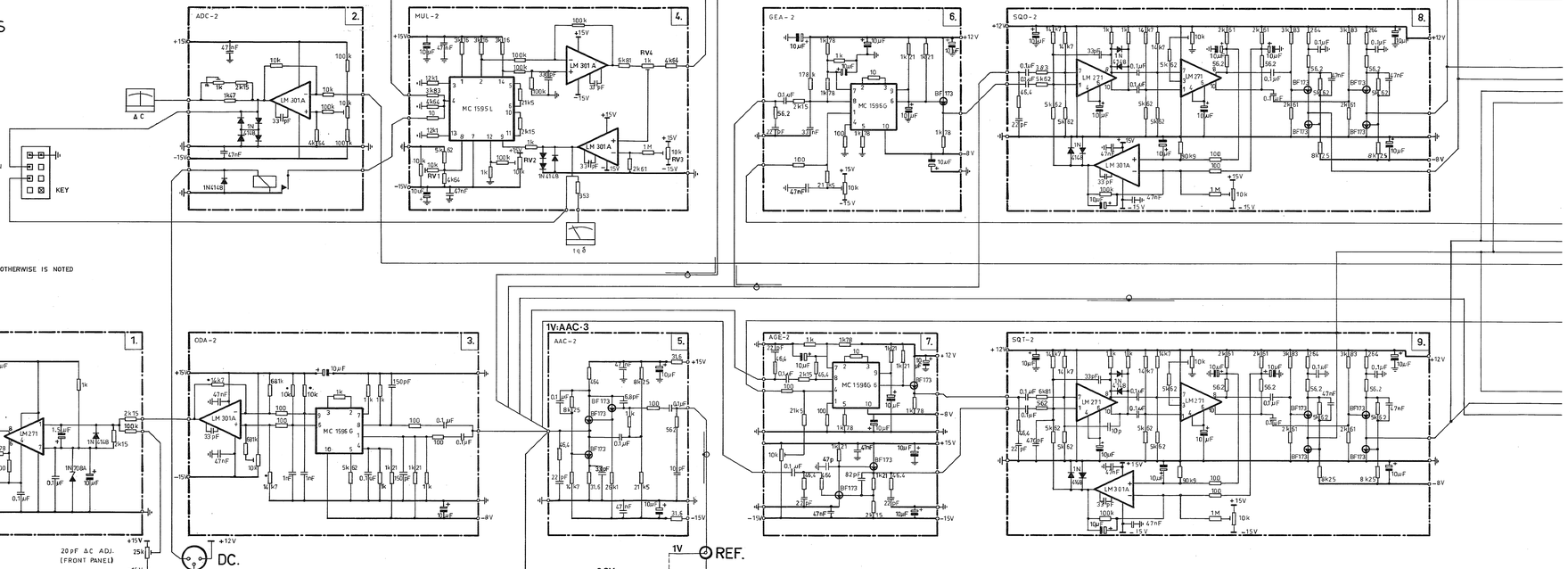


72361 - 19	CDB1-B1 DIAGRAM NO. 19	3 310377 BR	2 271175 BR	1	
A/S DANBRIDGE.	BRIDGE CIRCUIT	RETTET	220176	GODK.	
		TEGNET		080673 B. Rot	
		KONSTR		VAGN JENSEN	
		GODK			



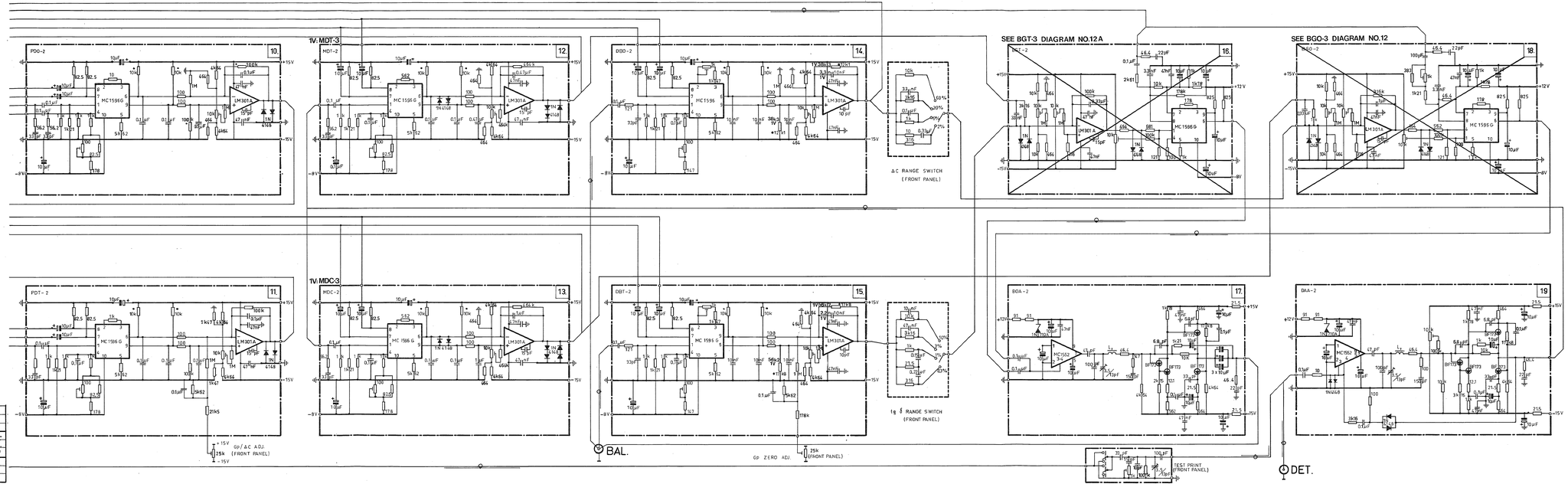
72360-20	CDB 1 DIAGRAM NO.20		
A/S DANBRIDGE	POWER SUPPLY	2912768 PFS	
		RETTET GODK.	
		TEGNET	020676 B.Ras.
		KONSTR.	J.W. HANSEN.
		GODK.	PFS

MAIN FRAME ELECTRONICS



72360 - 21	CDB1 ELECTRONICS	DIAGRAM NO. 21	
A/S DANBRIDGE.			

RETTET	2410808R	GODK.	
RETTET.	170878BR	GODK.:	
RETTET.	100674 B.R.	GODK.:	
RETTET:	210174 B.R.	GODK.:	
TEGNET.		150373 B.Ras.	
KONSTR.		J.W. HANSEN	
GODK.			



		RETTET	151080BR	GODK.
		RETTET	170818BR	GODK.
		RETTET	100574 BR	GODK.
		RETTET	050076 BR	GODK.
		TEGNET	150373 B.Pors	
		KONSTR.	J.W. HANSEN	
		GODK.		

72360-21	CDB1 DIAGRAM NO. 21	
A/S DANBRIDGE	ELECTRONICS	